

HL4A5/HL5A5 AMD Cezanne FP6 Logic Schematics

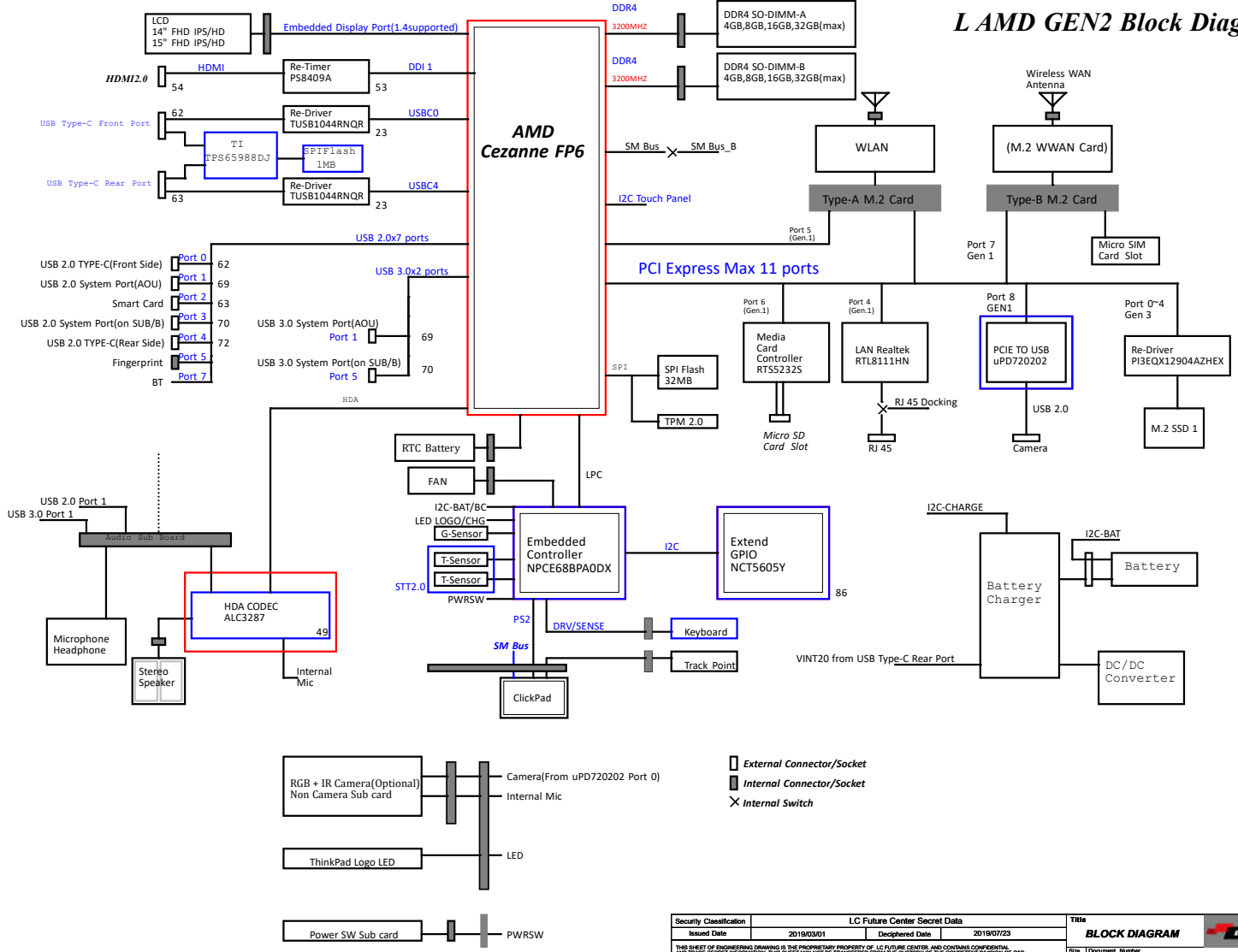
NM-D391

VER 0.1  
June.12.2020

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13.FP6(K)(L)(M) GND	48.BLANK	83.AUDIO BEEP	119.BLANK
14.DECAP_VDDCR_VDD MLCC	49.BLANK	84.AUDIO DEBUG	120.BLANK
15.DECAP_VDDCR_SOC MLCC	50.BLANK	85.EC_NPCE68APA0DX(1/2)	121.BLANK
16.BLANK	51.LCD CAMERA/MIC/TOUCH	86.EC_NPCE68APA0DX(2/2)	122.BLANK
17.BLANK	52.BLANK	87.BLANK	123.BLANK
18.BLANK	53.HDMI Re-Timer	88.KEYBOARD/TRACK POINT	124.LOAD SW PCH SUS
19.BLANK	54.HDMI CONNECTOR	89.TOUCH PAD/NFC/FPR	125.BLANK
20.RTC BATTERY	55.BLANK	90.FAN CONNECTOR	126.BLANK
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23.DOCK_USB/DP redriver2	58.PCie Re-driver-2	93.BLANK	
24.BLANK	59.THUNDERBOLT PD(TPS65988DJ)	94.BLANK	
25.BLANK	60.BLANK	95.BLANK	
26.BLANK	61.BLANK	96.BLANK	
27.BLANK	62.DOCKING CONNECTOR	97.BLANK	
28.PCIE_USB_Controller	63.TYPE-C CONNECTOR	98.DISCRETE TPM 2.0	
29.BLANK	64.M.2 SSD1	99.SCREW HOLES	
30.BLANK	65.BLANK	100.DC-IN	
31.BLANK	66.M.2_WLAN	101.BATTERY INPUT	
32.BLANK	67.M.2_WWAN_SOCKET	102.BATTERY CHARGER(BQ25700)	
33.DDR4 SUB CHANNEL-A	68.BLANK	103.DC/DC VCC5M (LV6228C)	
34.DDR4 SUB CHANNEL-A	69.USB3 AOU CONN	104.DC/DC VCC5M_PD(LV6228C)	
35.DDR4 SUB CHANNEL-B	70.BTB_CONN	105.DC/DC VCC3M (SYX198B)	

Security Classification	LC Future Center Secret Data		File
Issued Date	2018/01/12	Discontinued Date	2018/01/12
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# L AMD GEN2 Block Diagram



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Issued Date	2019/03/01	Deciphered Date	2019/07/23	<b>BLOCK DIAGRAM</b>	
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STATE	SIGNAL	SLP_S3#	SUSP#	SLP_S5#	BYSON	EC_ON
S0		HIGH		HIGH		ON
S3 (Suspend to RAM)		LOW		HIGH		ON
S4 (Suspend to Disk)		LOW		LOW		ON
S5 (Soft OFF)		LOW		LOW		ON

USB2 Port

Port	Device
0	Type-C front
1	USB3.0 AOU
2	SMART CARD
3	DB
4	Type-C rear
5	FPR
6	Camera
7	USB HUB

USB3 Port

Port	Device
0	Type-C front
1	Port1 AOU
4	Type-C rear
5	DB

PCIE Port

Port	Device
GPP0~3	SSD1
GPP4	LAN
GPP5	WLAN
GPP6	Card reader
GPP7	X
GPP8~9	NWAN
GFX0~7	X

Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane	VSYS15	VCC3M VCC5M VCC1R8_SUS VDD0R75	VCC1R2A VCC2R5A	VCC5B VCC3B VCC1R8B +0.75V8_VDDP VCC0R6B VDDCR_SOC VDDC_VDD
State				
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC Only	O	O	X	X
S5 S4 Battery only	O	X	X	X
G3 AC & Battery don't exist	X	X	X	X

SMBUS Control Table

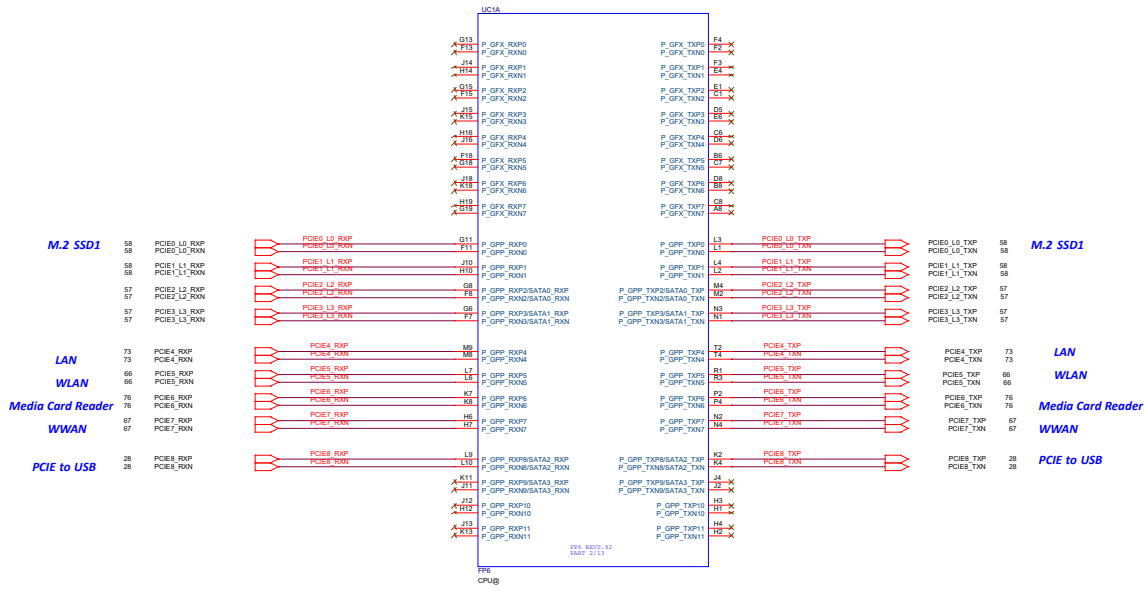
Schematic	SOURCE	TP	LAN	BATT	Charge	HUB	APU	USBC Retime	G-Sensor	Thermal Sensor	SODIMM	CP Module	NFC
SMB03_CLK SMB03_DATA	EC VCC3B	X	X	X	X	X	X	X	V VCC3B	V VCC3B	X	X	X
I2C_CLK_MUX I2C_DATA_MUX	EC VCC3SW_EC	X	X	X	X	X	X	V VCC3_SUS	X	X	X	X	X
I2C_CLK_BT I2C_DATA_BT	EC VCC3SW_EC	X	X	V	V	X	X	X	X	X	X	X	X
SMB0_CLK SMB0_DATA	APU VCC3B	X	X	X	X	X	V VCC3B	X	X	X	V	V	X
SMB1_CLK SMB1_DATA	APU VCC3M	V	V	X	X	V	V VCC3M	X	X	X	X	X	X
I2C0_CLK I2C0_DATA	APU VCC3B	X	X	X	X	X	V VCC3B	X	X	X	X	X	V

PD Controller I2C

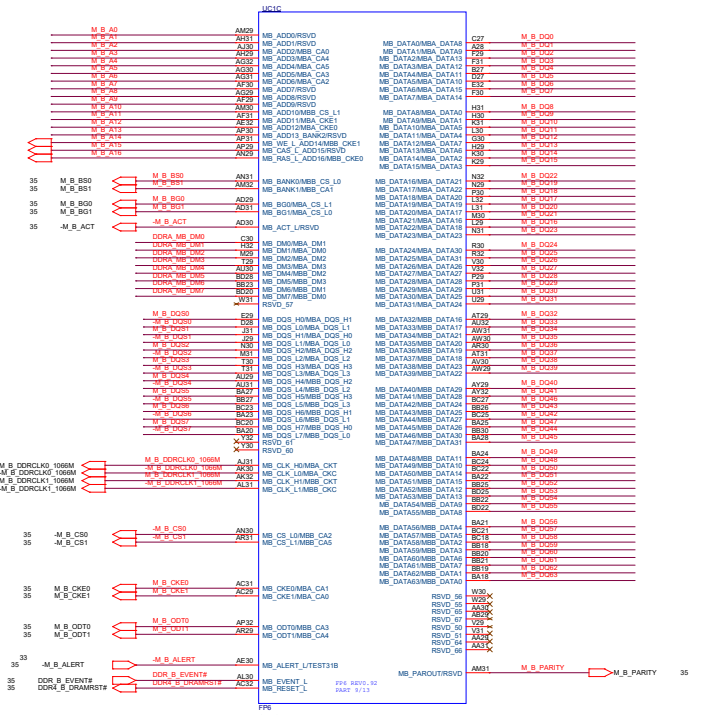
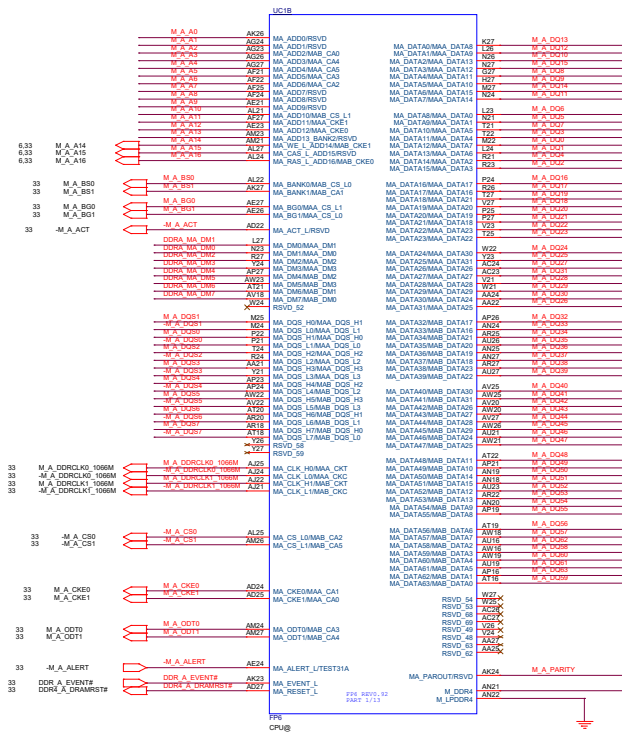
	SOURCE	APU
USBC_PD_I2C_SCL USBC_PD_I2C_SDA	PD VCC3_LDO_PD	V VCC1R8_SUS
I2C_CLK_TBT I2C_DATA_TBT	PD VCC3_LDO_PD	V VCC3B
I2C_CLK_PD I2C_DATA_PD	PD VCC3_LDO_PD	EC V VCC3SW_EC

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LCFC				114/L15 AND Gen
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Title		Memory DDR4	
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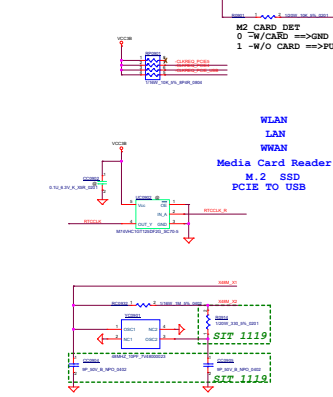


TABLE of Crystal (YCS)		
Vendor	LCFC P/N	Description
TAC	SJ10000000	5 CRYSTAL 48MHz 10PF +30PFM TV48000017
Siward	SJ10000000	5 CRYSTAL 48MHz 10PF XTLST1100-016

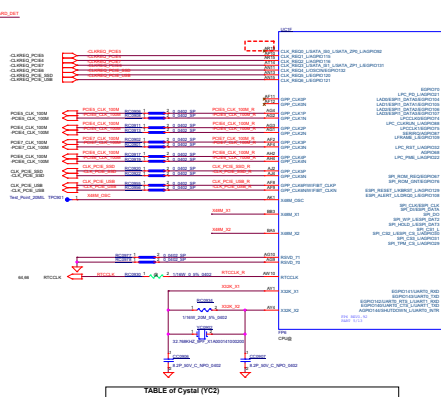
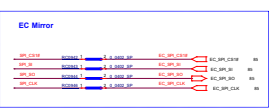
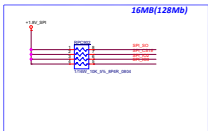
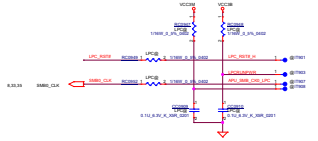
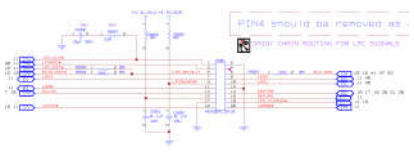


TABLE of Crystal (YCS)		
Vendor	LCFC P/N	Description
Siward	SJ10000000	5 CRYSTAL 32.768KHz 9PF XT1400F100000
Siward	SJ10000000	5 CRYSTAL 32.768KHz 9PF XTL721-150-008

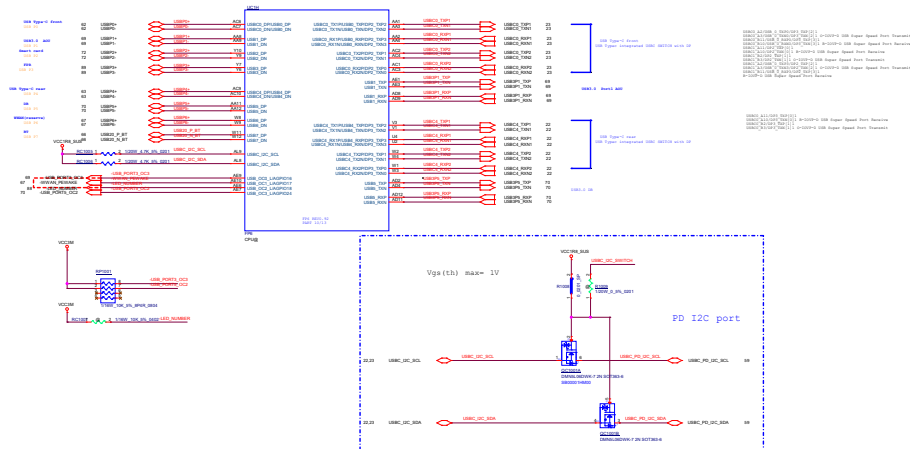


LPC debug connector 20PIN, only reserve test point  
As below is CRB circuit

LPC ROM EMULATOR HEADER



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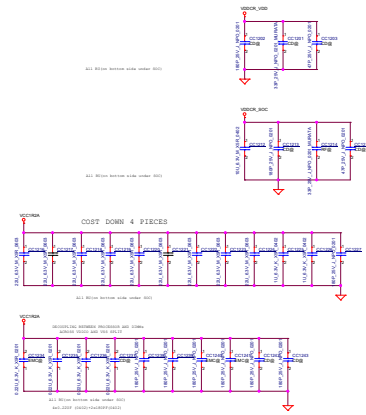
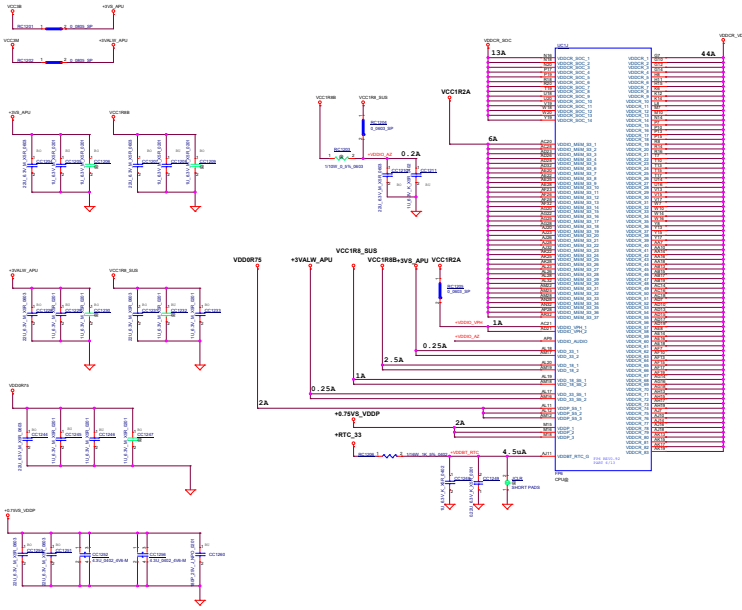


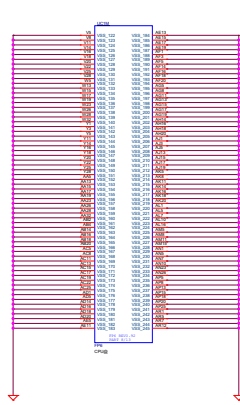
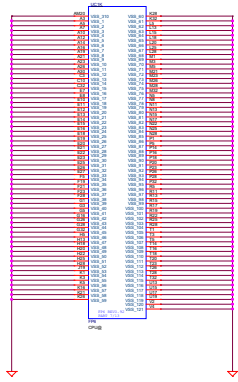
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Issued Date		Declassified Date		 <b>USB/WIFI</b>	
20100301		20100703		Date of Revision 1	

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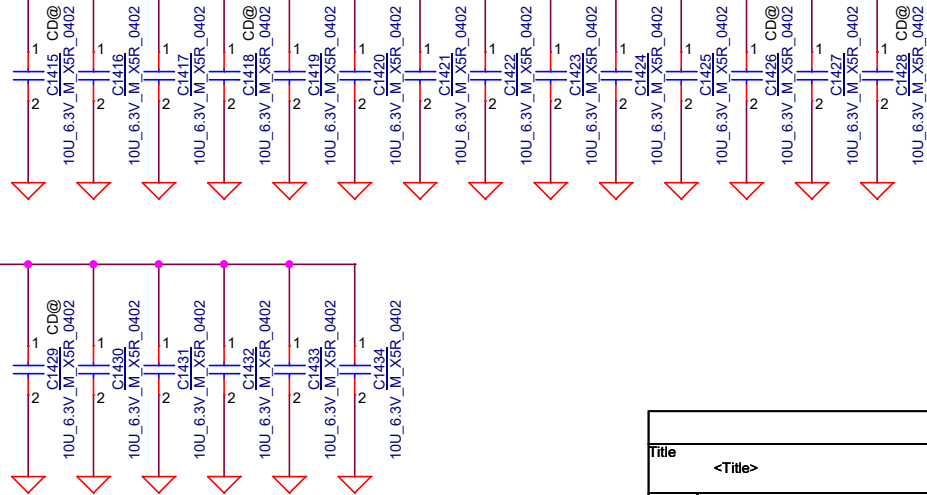




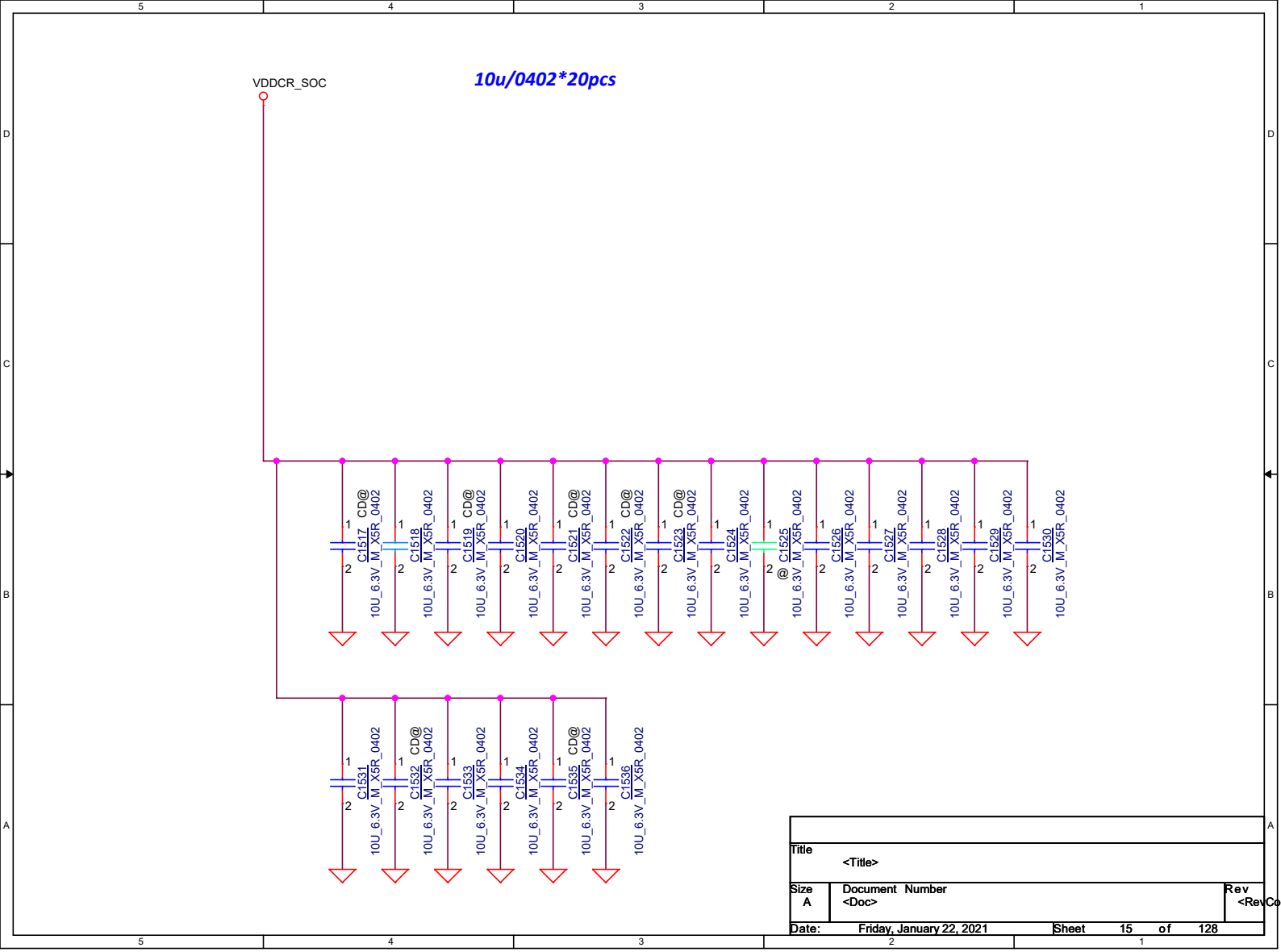
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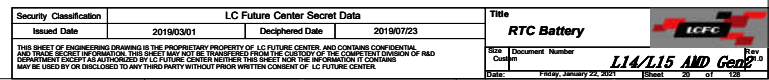
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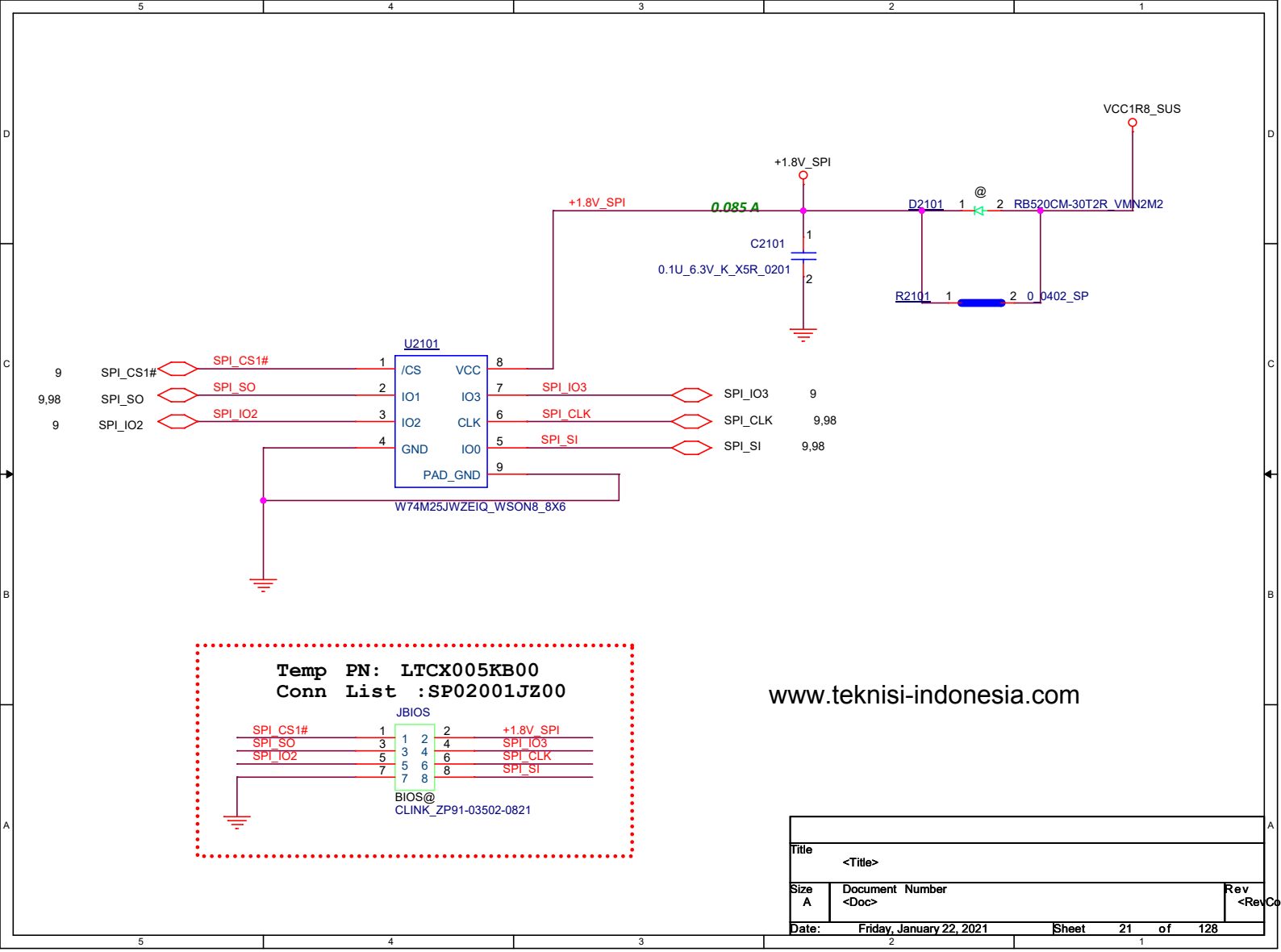
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Title	Author	Year	Journal	Volume	Issue	Page
1. The Effect of Temperature on the Rate of Reaction	John Doe	2018	Journal of Chemical Education	95	3	456-462
2. Kinetics of the Reaction Between Hydrogen Peroxide and Potassium Iodide	Jane Smith	2017	Journal of Chemical Education	94	2	234-240
3. The Effect of Concentration on the Rate of Reaction	Michael Brown	2016	Journal of Chemical Education	93	1	123-129
4. The Effect of Surface Area on the Rate of Reaction	Sarah White	2015	Journal of Chemical Education	92	4	567-573
5. The Effect of Catalysts on the Rate of Reaction	David Green	2014	Journal of Chemical Education	91	5	678-684

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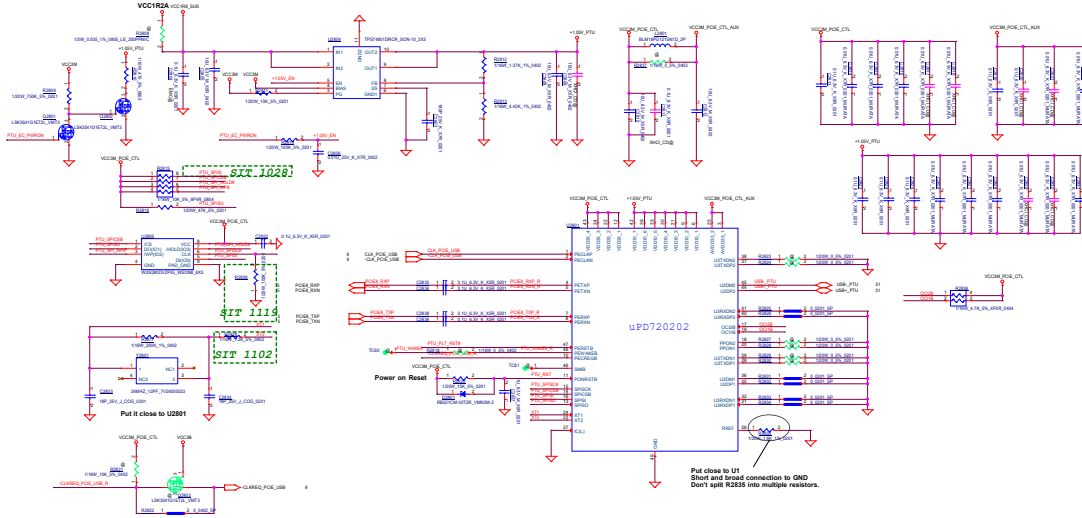
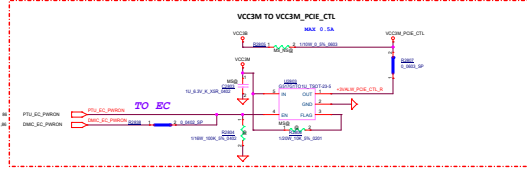
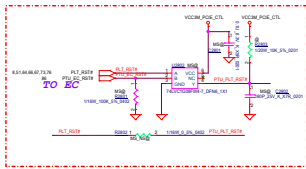
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PCE TO USB CONTROLLER			11/2/11

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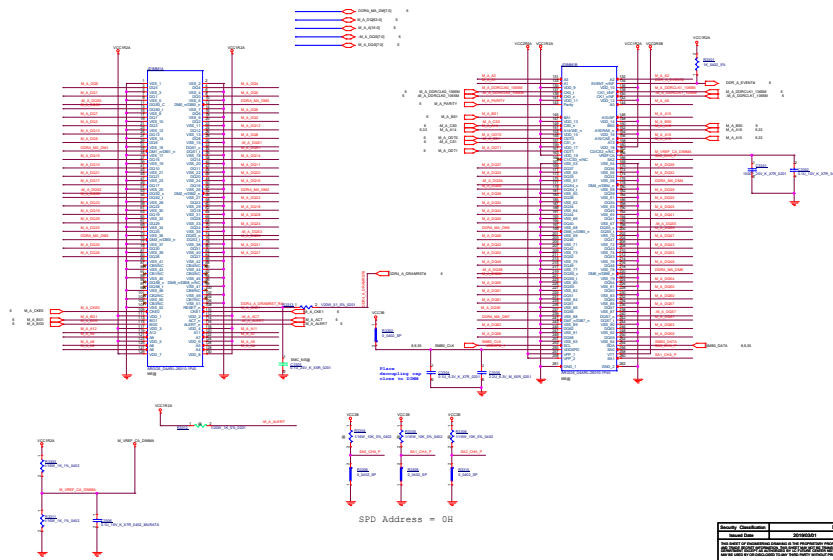
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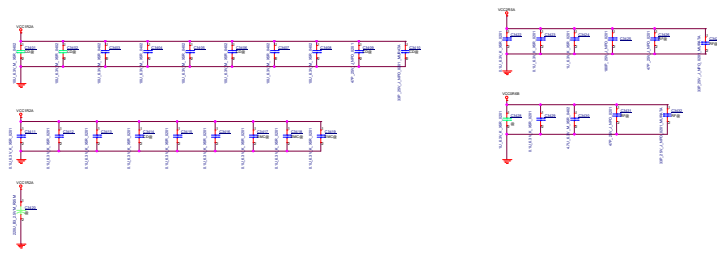
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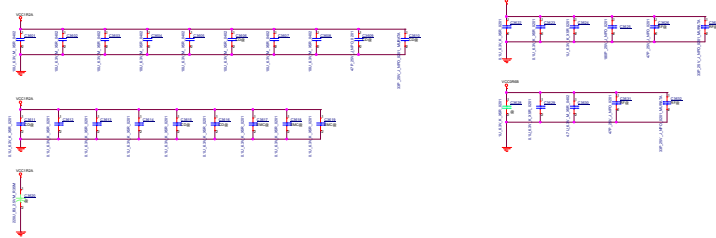




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1.0	2018/01/11	Initial Release	2018/01/11	Initial Release	







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2. Kinetics of the Reaction Between Hydrogen Peroxide and Potassium Iodide	Jane Smith	2016	Journal of Chemical Education	93	1	123-129
3. The Effect of Concentration on the Rate of Reaction	Michael Brown	2017	Journal of Chemical Education	94	2	234-240
4. The Effect of Surface Area on the Rate of Reaction	Sarah White	2018	Journal of Chemical Education	95	4	567-573
5. The Effect of Catalysts on the Rate of Reaction	David Green	2019	Journal of Chemical Education	96	1	101-107

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1. The Effect of Temperature on the Rate of Reaction	John Doe	2018	Journal of Chemical Education	95	3	456-462
2. Kinetics of the Reaction Between Hydrogen Peroxide and Potassium Iodide	Jane Smith	2017	Journal of Chemical Education	94	2	321-328
3. The Effect of Concentration on the Rate of Reaction	Michael Brown	2016	Journal of Chemical Education	93	1	123-130
4. The Effect of Surface Area on the Rate of Reaction	Sarah White	2015	Journal of Chemical Education	92	4	567-574
5. The Effect of Catalyst on the Rate of Reaction	David Green	2014	Journal of Chemical Education	91	5	678-685

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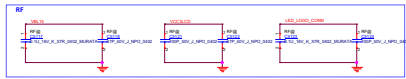
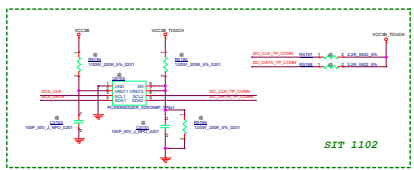
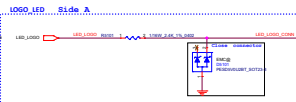


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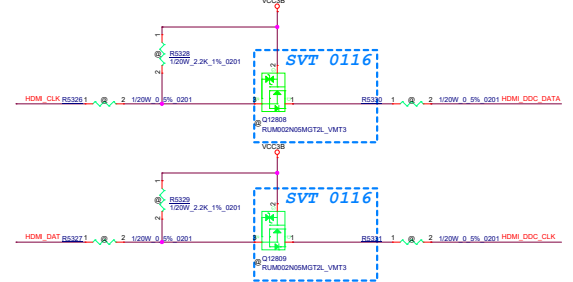
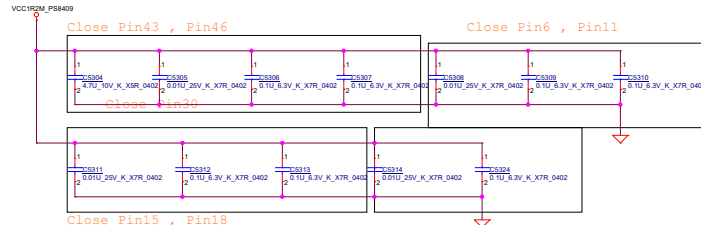
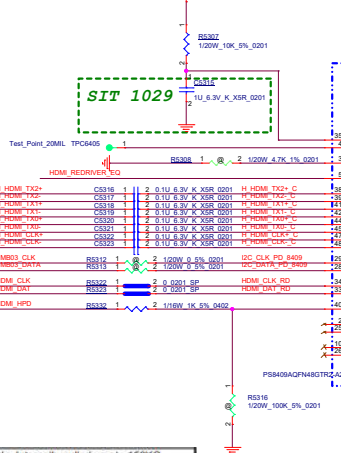
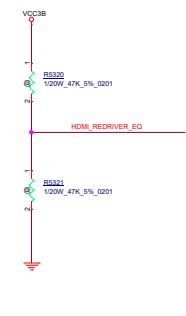
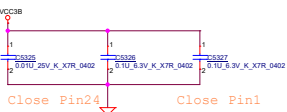
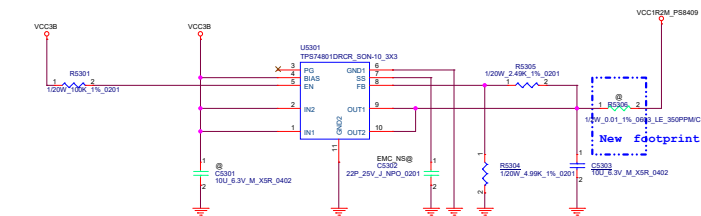


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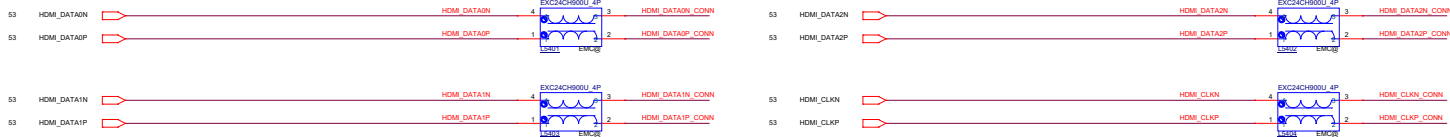
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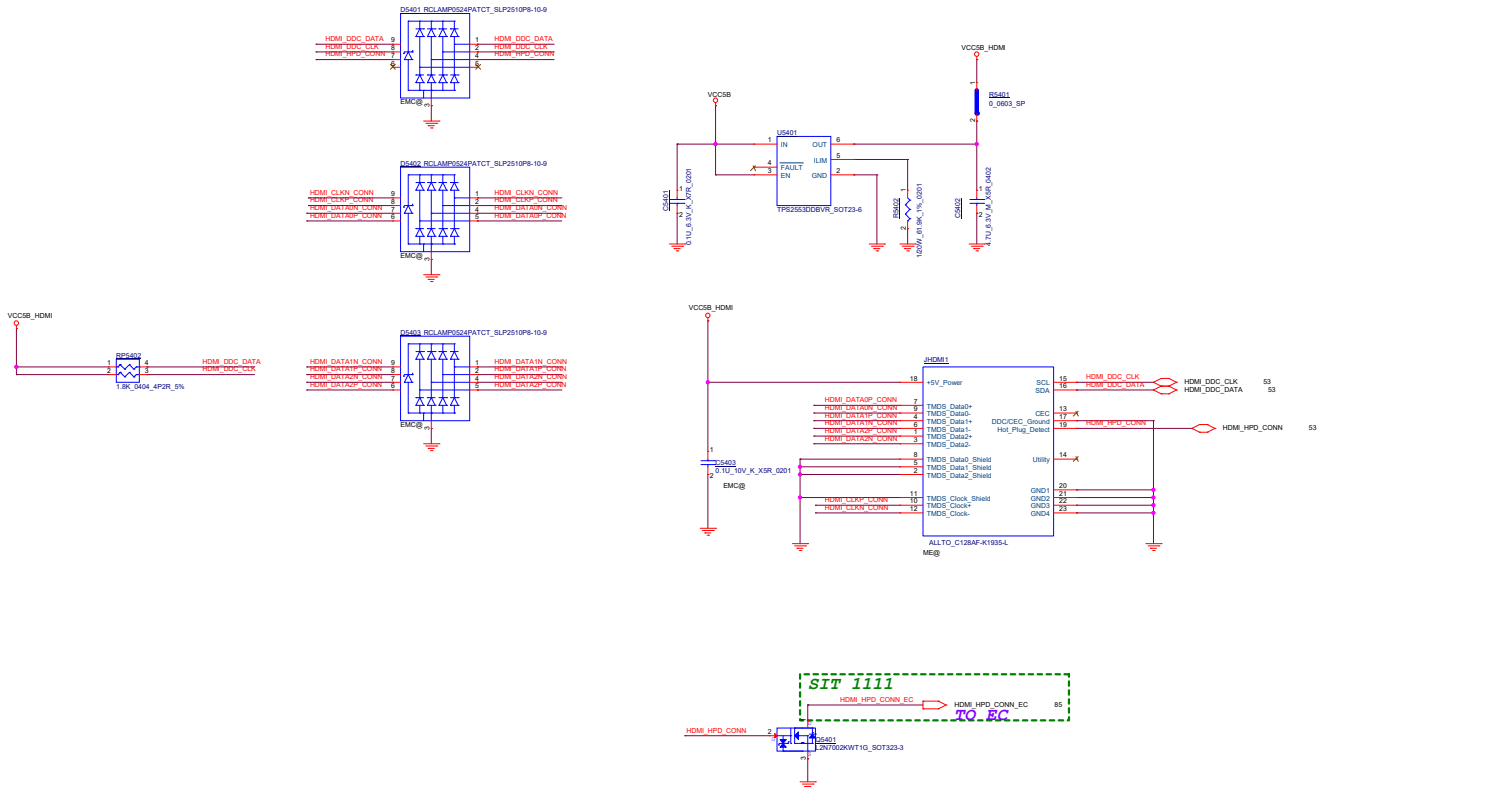


3	DCIN_ENB	LVTTTL	I	DC coupling enable. Internally pulled up at ~150KΩ. L: DC coupling input H: AC coupling input(default)
5	EQ	LVTTTL	I	Receiver equalization setting. Internally pulled up at ~150KΩ. L: Programmable EQ for channel loss up to 15.6dB H: Programmable EQ for channel loss up to 17.9dB(default) M: Programmable EQ for channel loss up to 11dB
27	PRE	LVTTTL	I	Output pre-emphasis setting. Internally pulled up at ~150KΩ. L: Programmable pre-emphasis to 2.5dB H: No pre-emphasis (default)

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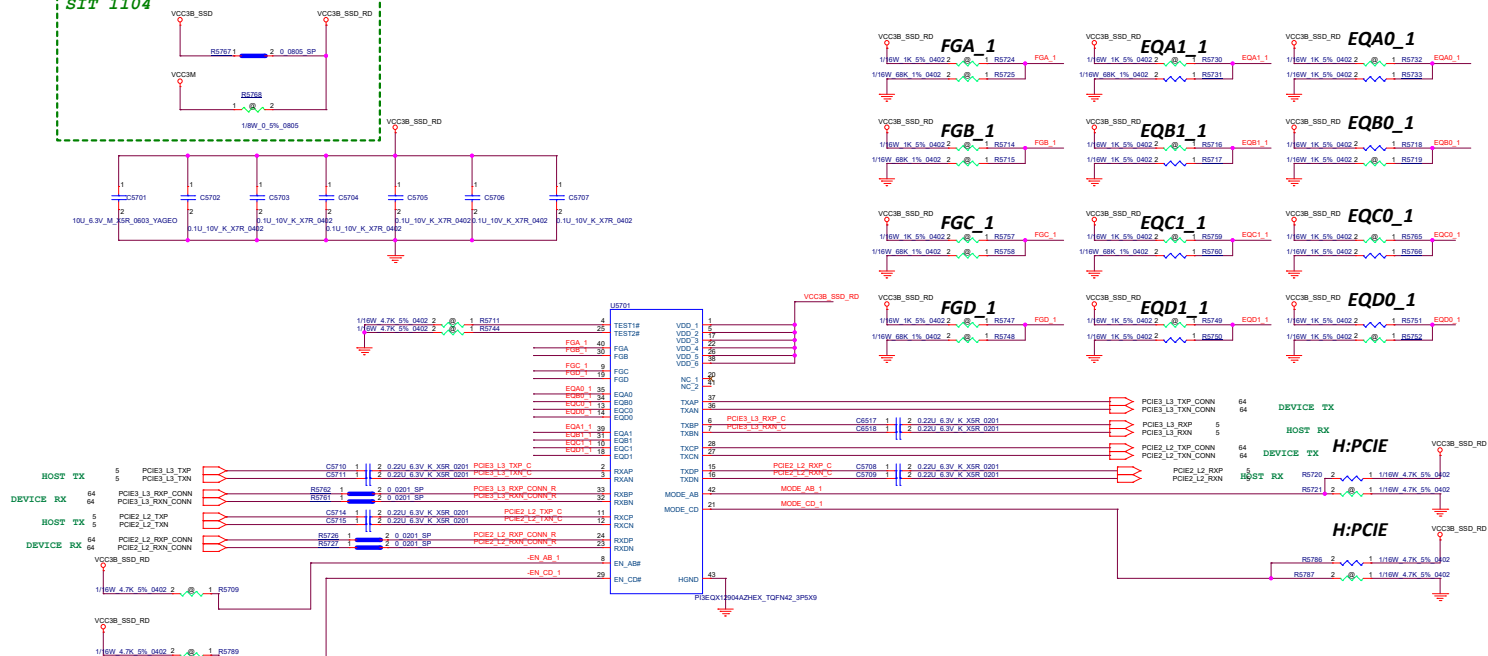
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EL480/580 Setting						
TX EQ	TX SW	TX Gain		RX EQ	RX SW	RX Gain
A1:R A0:F	1	F		B1:0 B0:1	1	F
TX EQ	TX SW	TX Gain		RX EQ	RX SW	RX Gain
A1:R A0:F	1	F		B1:0 B0:1	1	F

For 12902A:

0 means , pull down to GND thru 1K ohm  
 F, Floating  
 1 , pull up to VDD thru 1K ohm  
 R , pull down to GND thru 68K ohm.

Channel Enable Setting	
EN#	Setting
0	Enabled (Default)
1	Disabled

## Equalization Setting:

EQ/A/B are the selection pins for the equalization selection

EQ		Equalizer setting (dB)			
A1/B1	A0/B0	@1.25GHz	@2.5GHz	@3GHz	@4GHz
0	0	0.4	1.8	2.4	3.9
0	R	0.6	2.3	3.2	4.9
0	F	0.8	2.9	3.9	5.8
0	1	1.0	3.5	4.6	6.6
R	0	2.1	4.4	5.3	7.2
R	R	2.3	4.9	5.9	7.9
R	F	2.5	5.3	6.4	8.5
R	1	2.7	5.8	7.0	9.1
F	0	3.7	6.5	7.7	9.7
F	R	3.9	6.9	8.1	10.2
F	F	4.1	7.3	8.5	10.6
F	1	4.3	7.6	8.9	11.0
1	0	5.4	8.4	9.5	11.4
1	R	5.6	8.7	9.8	11.8
1	F	5.8	9.0	10.2	12.1
1	1	5.9	9.2	10.4	12.5

## Flat Gain Setting:

FGA/B are the selection bits for the DC gain.

Flat Gain Settings	
FGA/B	dB
0	-3.5
R	-1.5
F	0 (Default)
1	+1.5

## -1dB compression point output Swing Setting:

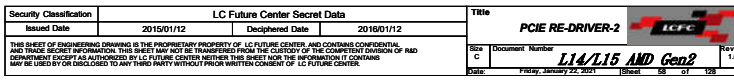
SWA/B are the selection bits for the -1dB compression point output swing setting (100MHz)

Output Linear Swing Settings	
SWA/B	mVpp
0	900
R	1050
F	1000 (Default)
1	1120

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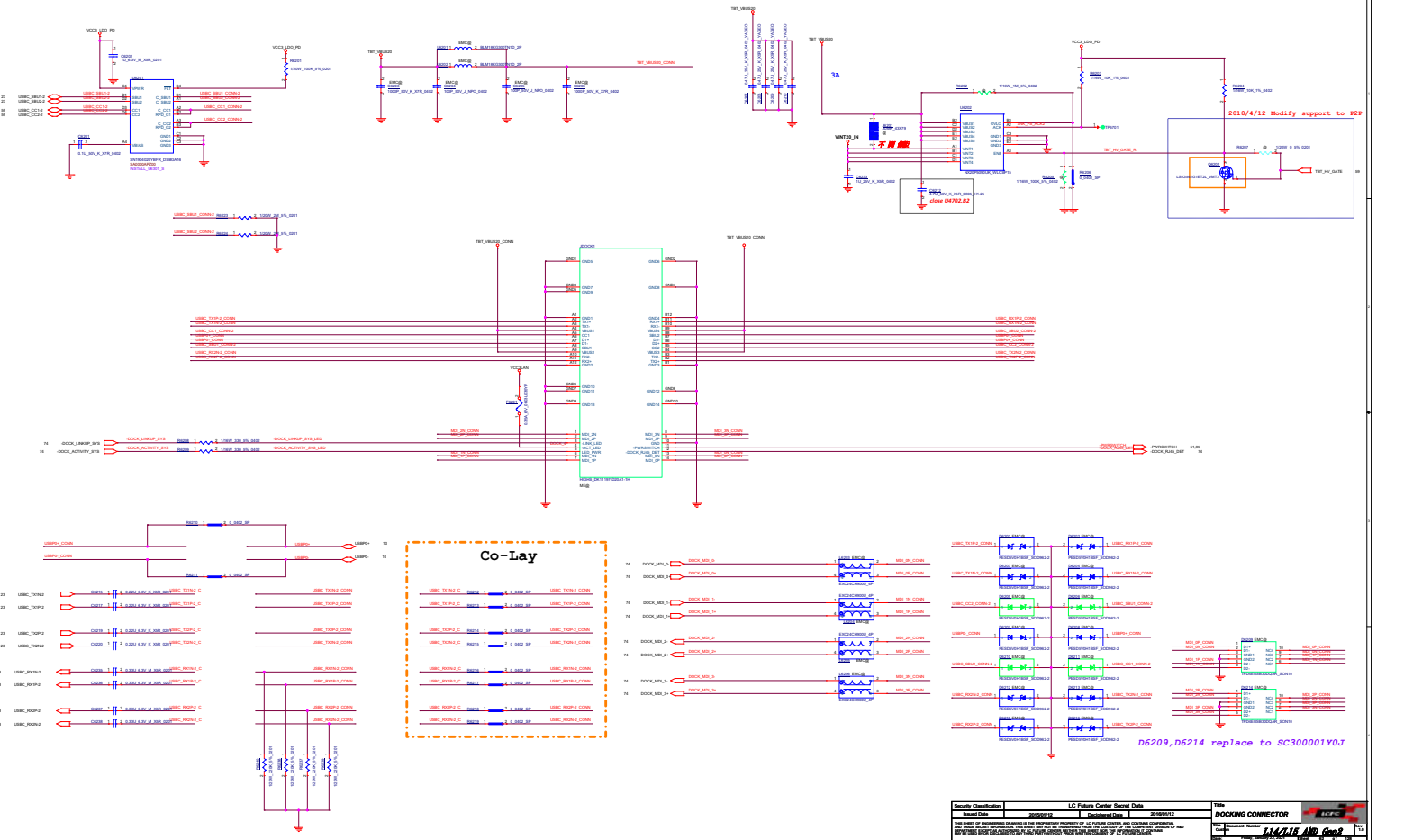




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Date:	Friday, January 22, 2021			Sheet 61 of 128																													
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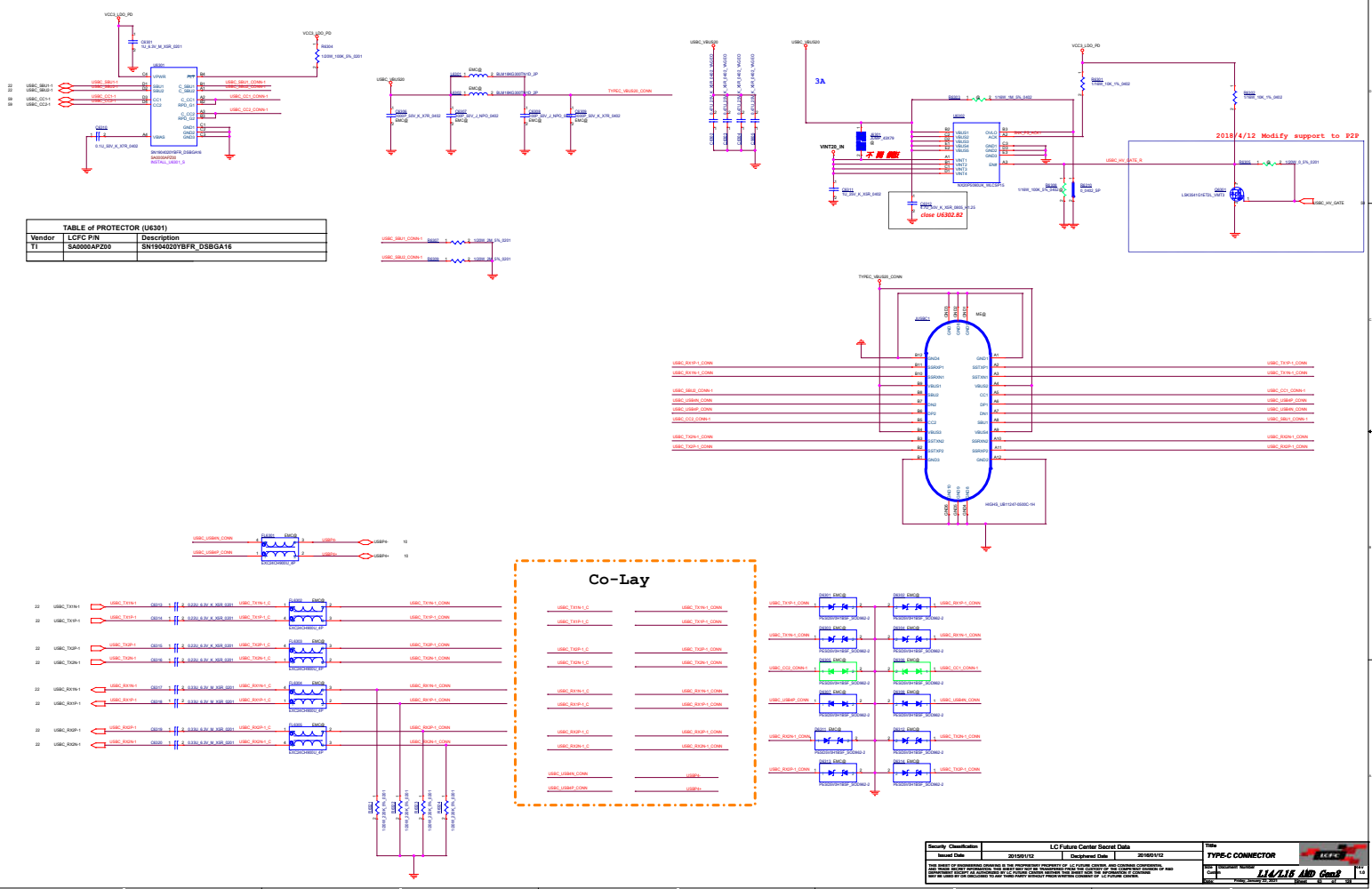


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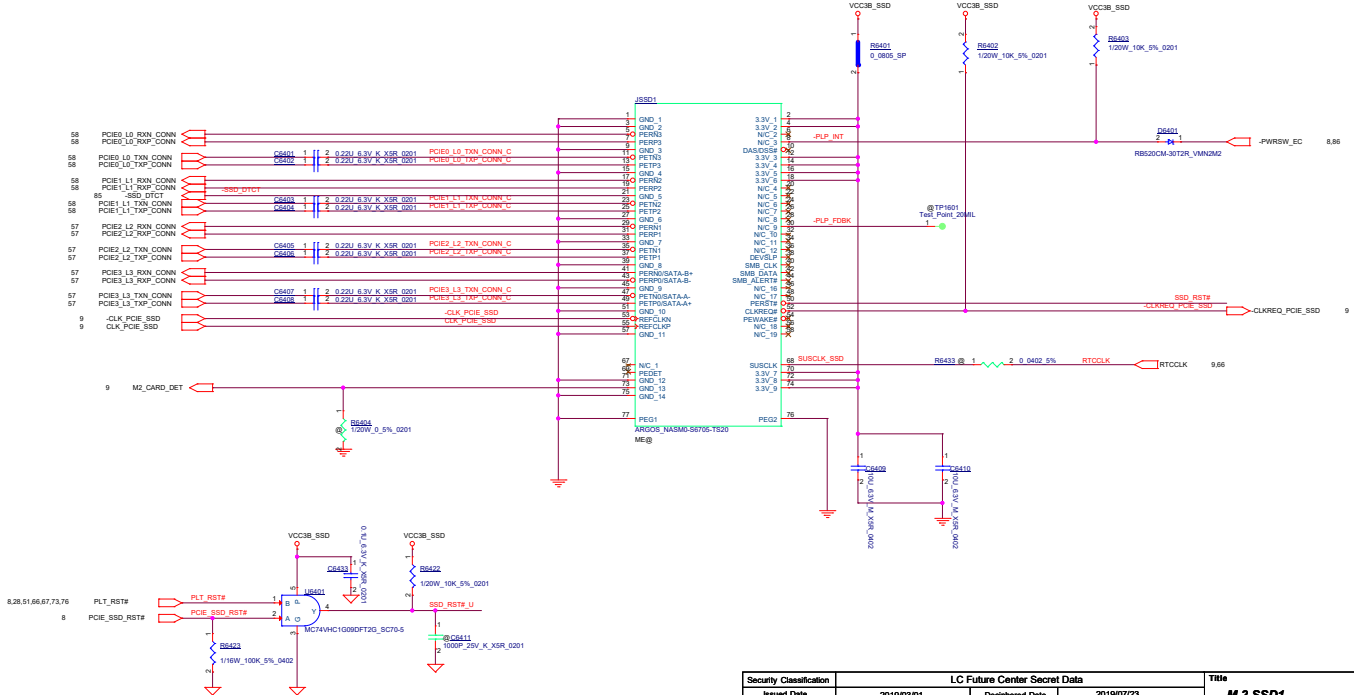
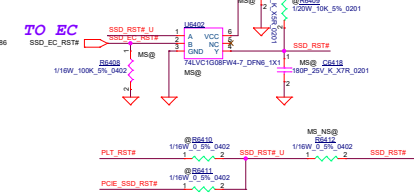
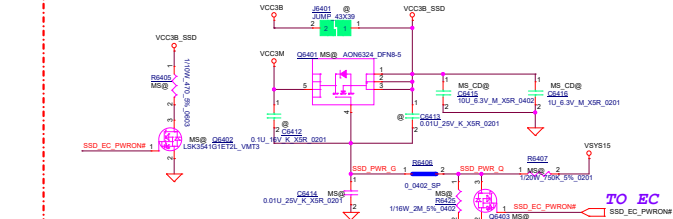
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Classified Date	2019/11/12	Declassified Date	2019/11/12		TYPE-C CONNECTOR	
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SSD0001100U ADM324 18 0P9-8  
Load MOS N MOS Id <= 30A, Vgs(th) Max >= 2V  
Vds max 30V, Vgs Max @20, Rise(fcn) >= 3, fmax

9V--13.6V MAX 3A  
SSD Power control  
DYL@190426

SSD Reset control  
DYL@190426

New And gate push pull output  
PH need unstuff

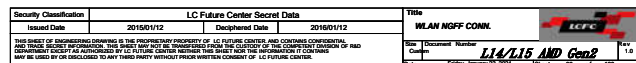


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Title			
M.2 SSD1			
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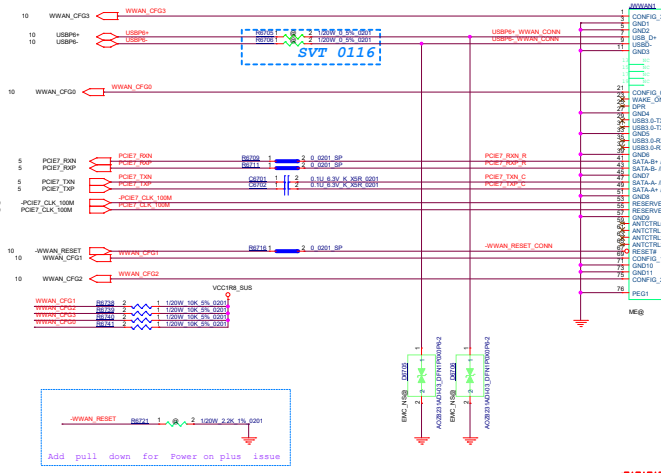
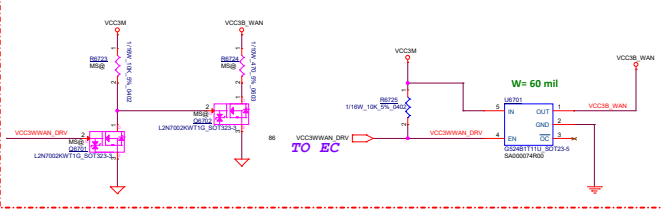
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			Document Number <b>L14/L15 AND Gen2</b>
			Rev. 0
			DATE: Friday, January 22, 2021 15:55:15



# M.2 Socket 2 (Key-B) for 3042 S3 WWAN H=2.00mm Connector

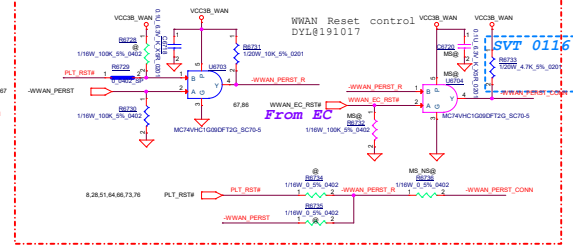
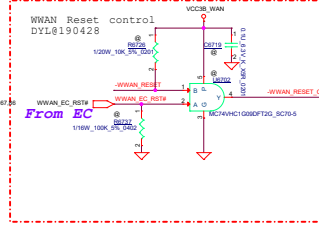
WWAN Power control  
DYL@190428



State #	CONFIG_0 (Pin 21)	CONFIG_1 (Pin 69)	CONFIG_2 (Pin 75)	CONFIG_3 (Pin 1)	Module Type and Main Host Interface	Module
	GND	GND	GND	NC	WWAN - PCIe, USB 3.1 Gen1	Quectel EM120R

Table 21: Pin Definition of Configuration Pins

Pin No.	Pin Name	I/O	Power Domain	Description
21	CONFIG_0		0	Connected to GND internally.
69	CONFIG_1		0	Connected to GND internally.
75	CONFIG_2		0	Connected to GND internally.
1	CONFIG_3		0	NC



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# USB AOU

VCC5M 25,51,70,72,78,84,85,103,106,107,108,109,110,127,128  
USB\_PWR\_S2

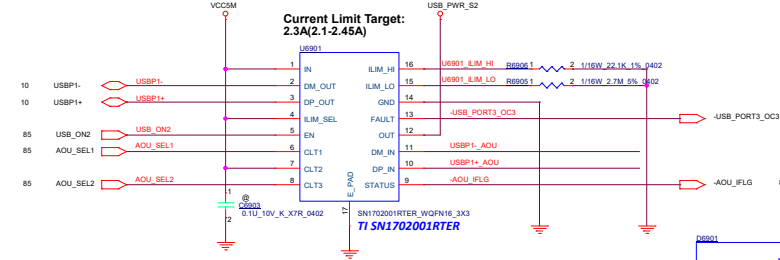
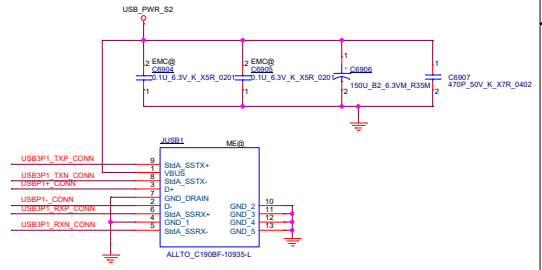
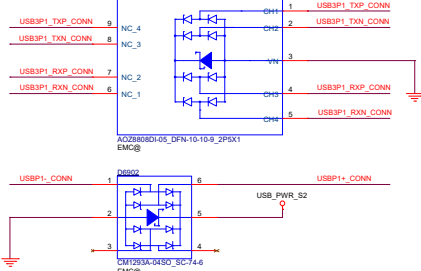


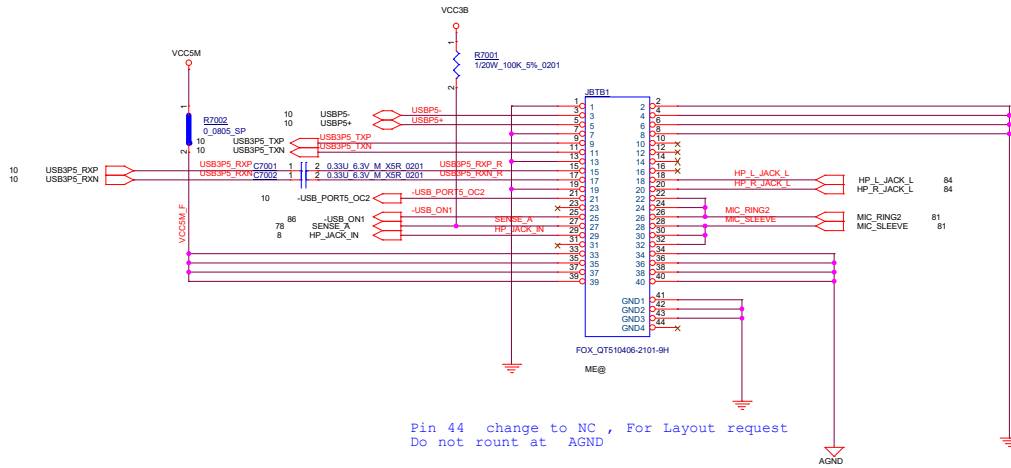
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DIODES	SA00009D800	S IC PI5USB2546H2HEX TQFN 16P CONTROLLER

CLT1	CLT2	CLT3	ILM_SEL	MOD
0	0	0	X	DCR OUT held low
1	1	1	1	CDP Data Connected and Port Power Mgt. Function Active
1	1	1	0	SDP2 Data Connected
1	1	0	X	SDP1 Data Connected
1	0	0	X	DCP_Short Device Forced to stay in DCP BC 1.2 charging mode
1	0	1	X	DCP_Divider Device Forced to stay in DCP Divider 1 Charging Mode
0	1	1	X	DCP_Auto Data Disconnected and Port Power Mgt. Function Active
0	0	1	X	DCP_Auto Data Disconnected and Power Wake Function Active



D6901 replace to SC300001Y0J

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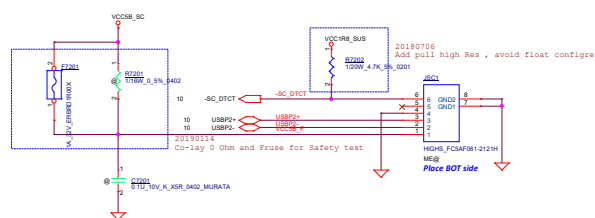
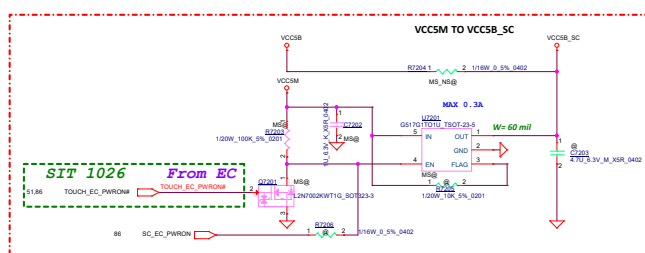



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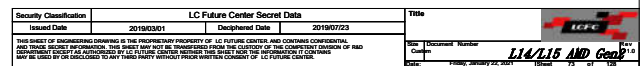
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**SMART CARD CONN.**



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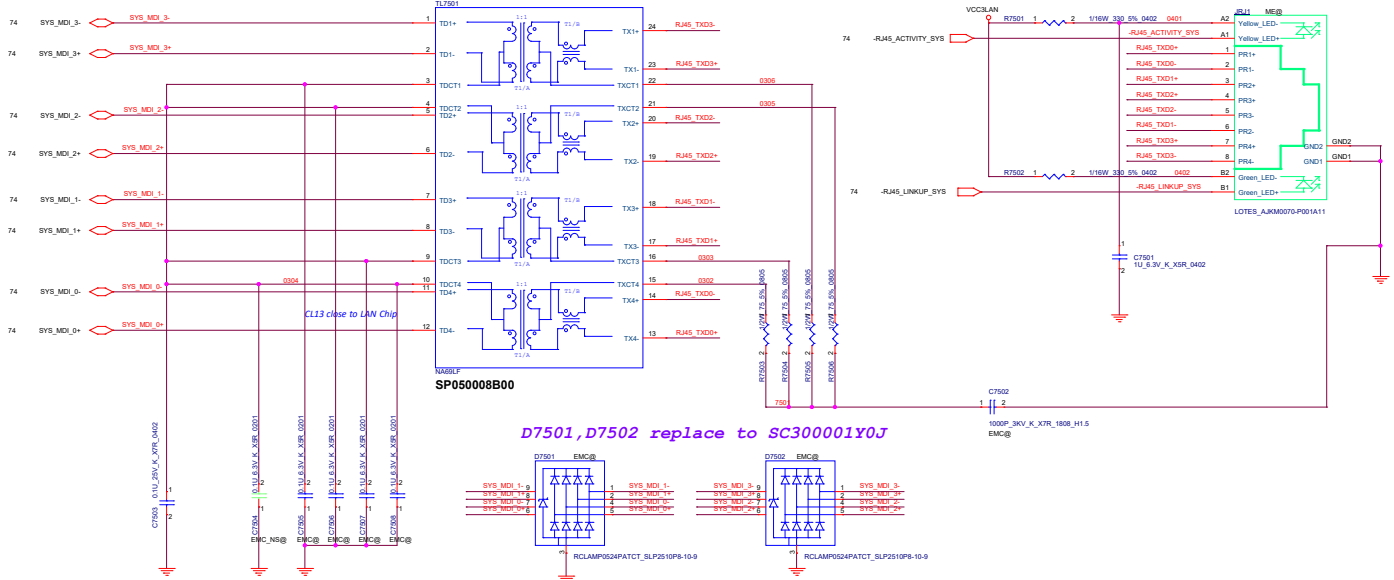





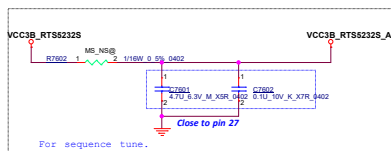
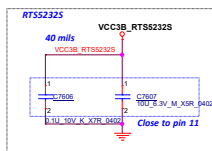
For L-Series

LAN X' FORM

RJ45 Conn.

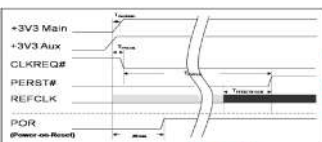
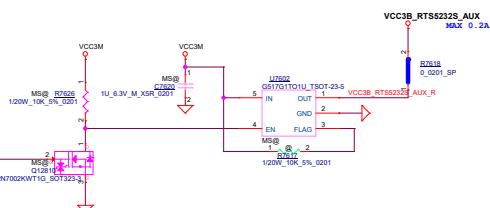


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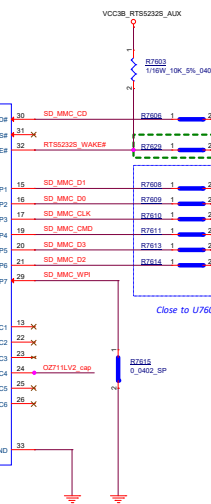
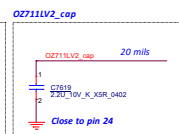
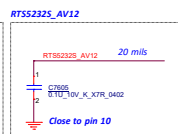
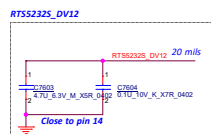
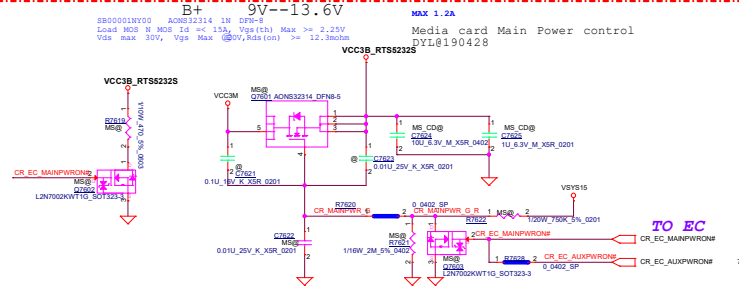
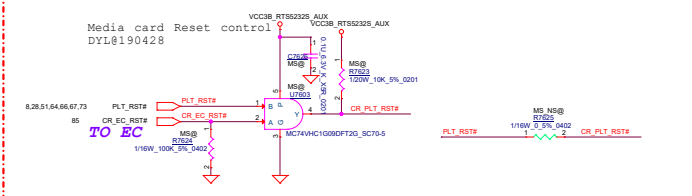
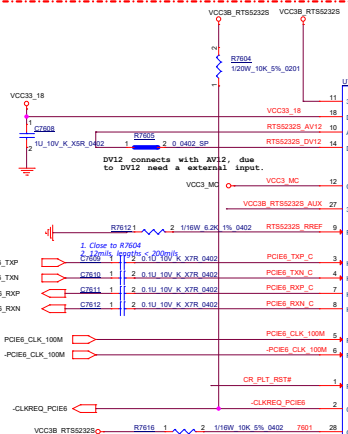


Media card AUX Power control  
DYL@190428

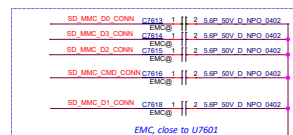
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DYL@190428



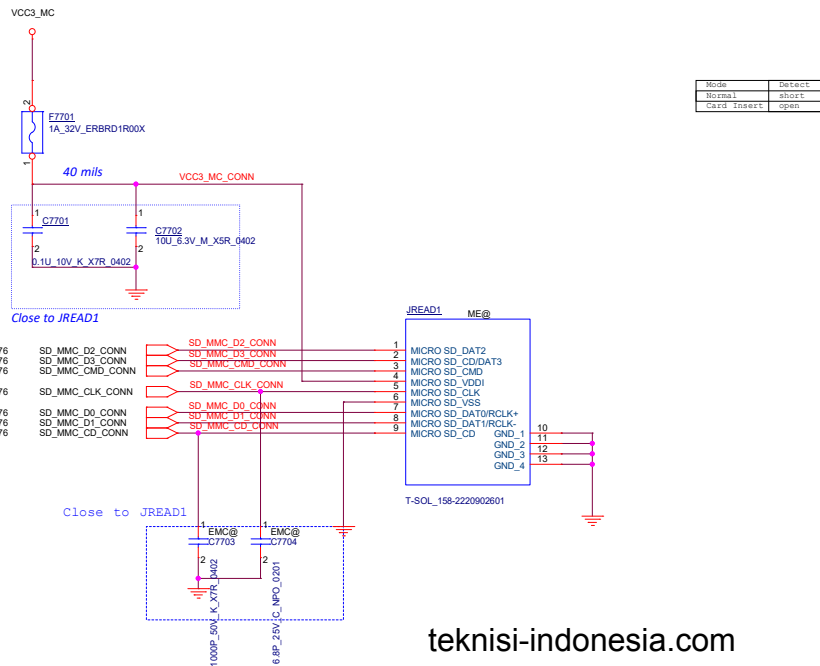
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SA00009F600	OZ711LV2LN-A-0-TR



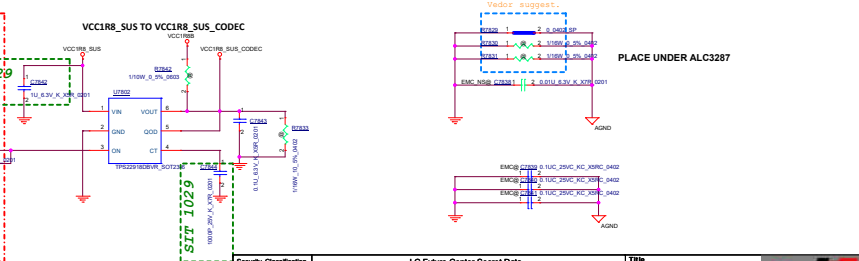
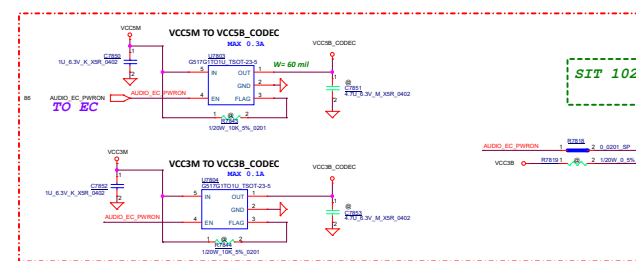
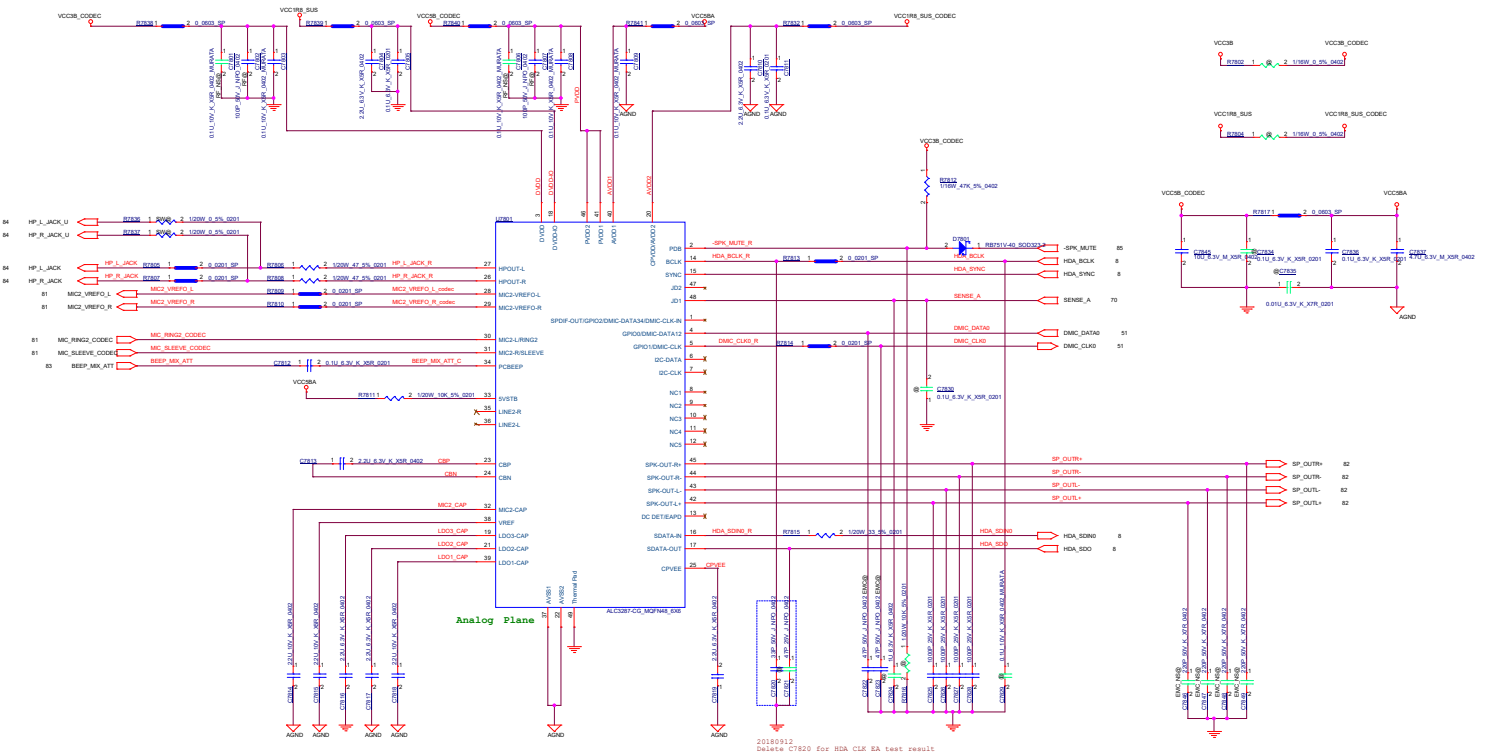
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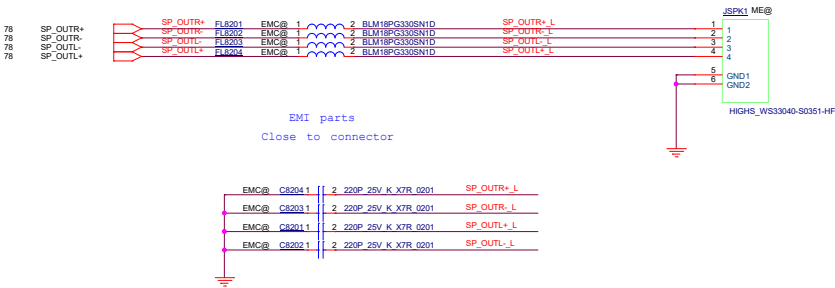
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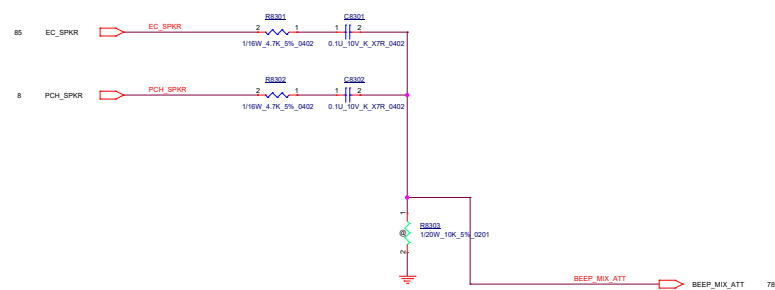



SPK CONN.



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Size	Document	Number	L14/L15 AMD Gen2	
Custom				
Date:	Friday, January 22, 2021	Sheet	82	of 128

Audio Beep

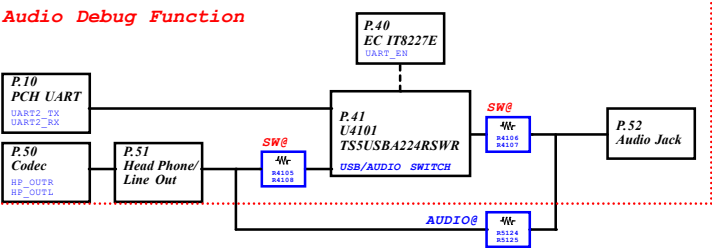


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0.5X		114/L15 AND Gen2		0	
Date		Project		Sheet	
2019/07/23		114/L15 AND Gen2		15	

FUNCTION TABLE

A <sub>SEL</sub>	V <sub>AUDIO</sub>	V <sub>BUS</sub>	L/R	D+, D-
L	L	L	OFF	OFF
L	L	H	OFF	OFF
L	H	L	ON	OFF
L	H	H	OFF <sup>(1)</sup>	ON
H	L	L	OFF	OFF
H	L	H	OFF	OFF
H	H	L	ON	OFF
H	H	H	ON	OFF

(1) 100Ω shunt resistors are enabled in this state.



AUDIO DEBUG PORT

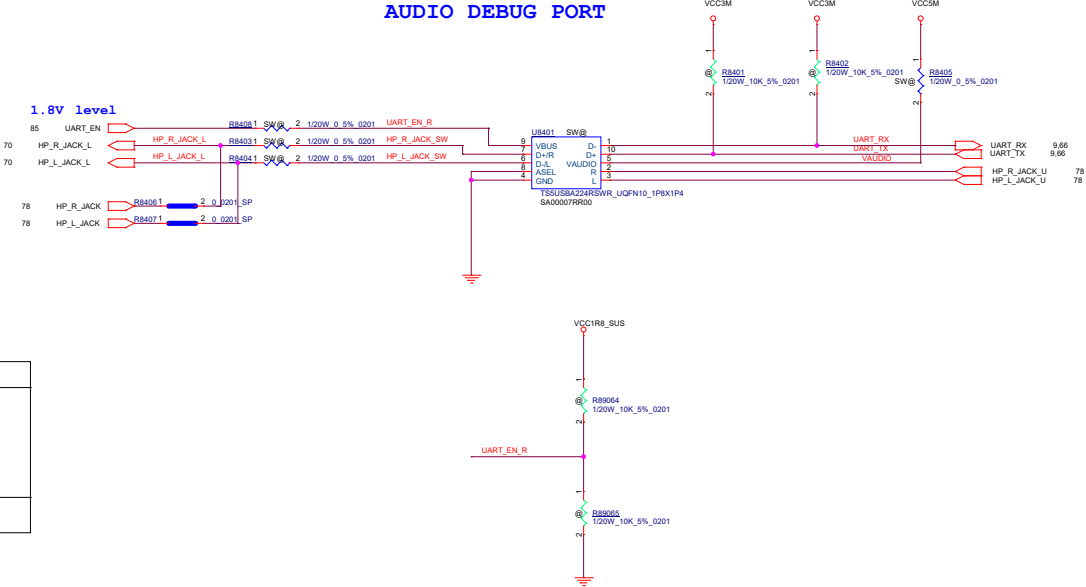
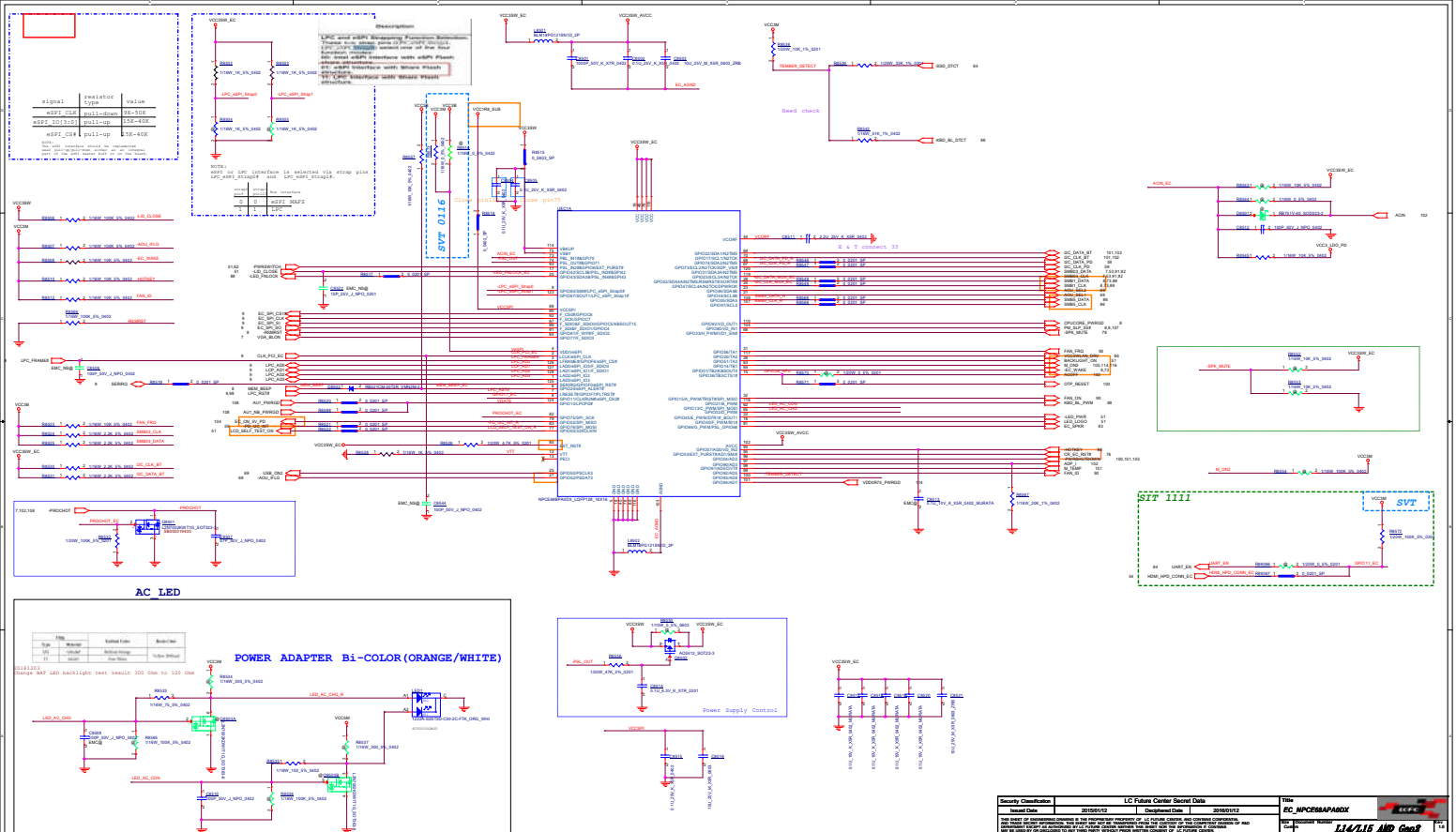


TABLE:

Mode	Audio	UART
UART_EN	L	H

TABLE:

Part Name	For NPI	For MP
U8401 SW#	ASM	NA
R8403 SW#	ASM	NA
R8404 SW#	ASM	NA
R8401 SW#	ASM	NA
R8402 SW#	ASM	NA
R8405 SW#	ASM	NA
R8506 AUDIO#	NA	ASM
R8507 AUDIO#	NA	ASM



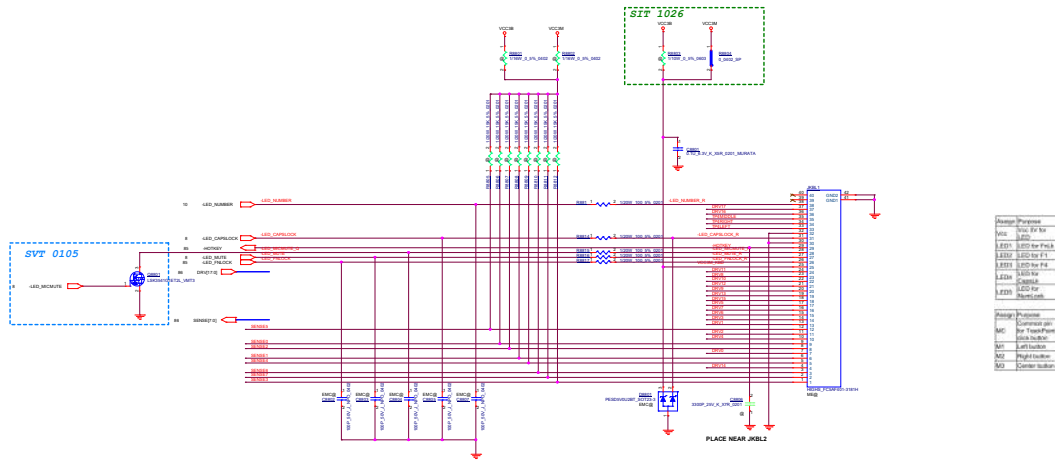
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Scale	Document Number		<b>L14/L15 AND Gen2</b>
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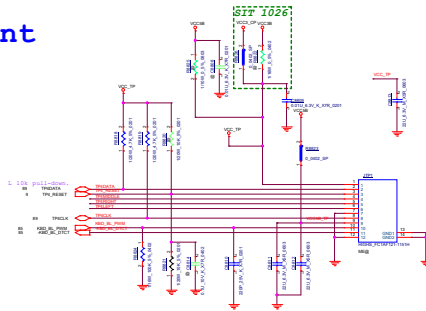
## Keyboard CONN



## Track Point

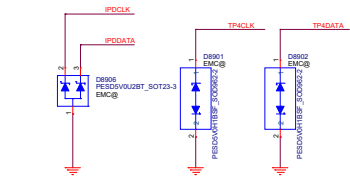
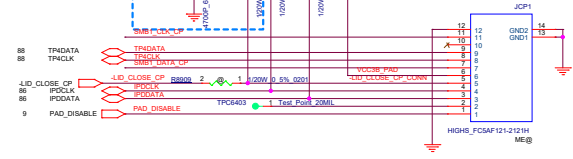
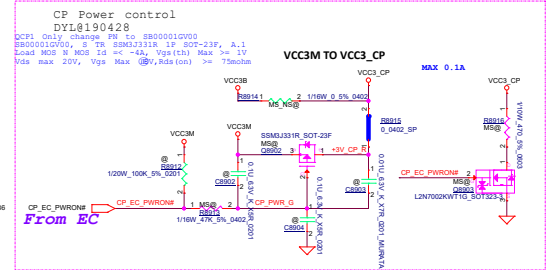
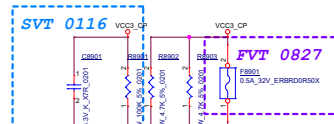
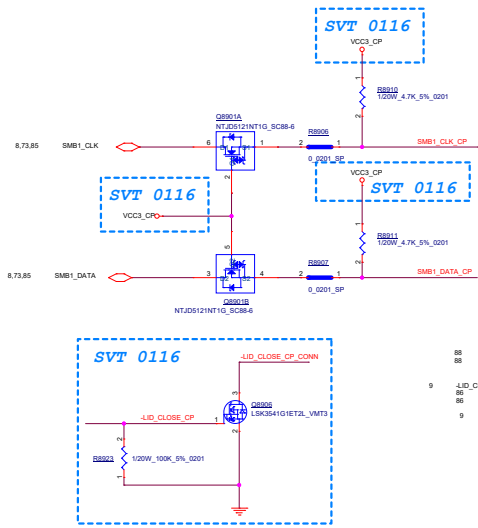
TrackPoint and Backlight FPC Pin Assignment

Pin #	Assign
1	VCC (3.3V)
2	IPD DATA
3	IPD RST
4	MIDDLE
5	RIGHT
6	LEFT
7	IPD GND
8	IPD CLK
9	LED VCC5 (5V)
10	LED PWM
11	Backlight detection
12	LED GND

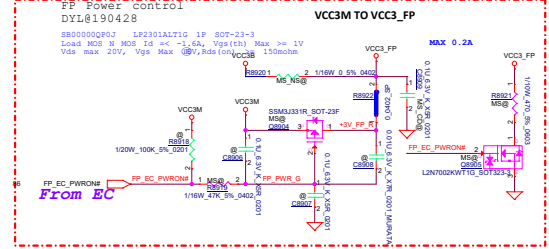
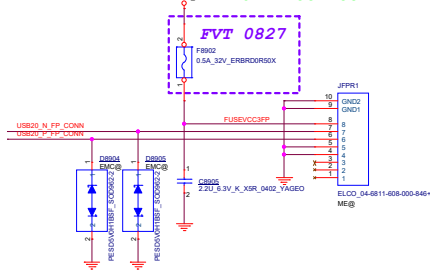
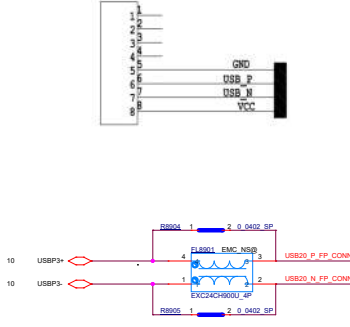




# Click Pad For L-Series



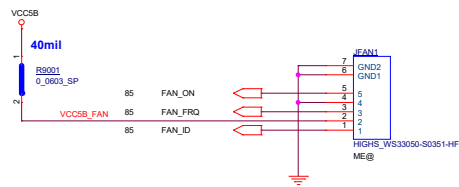
# FingerPrint Conn For L-Series



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Issued Date		Declassified Date		TOUCH PAD/NFC/FP	
2015/01/12		2018/01/12		Doc#	
2015/01/12		2018/01/12		114/L15 AND Gen2	
2015/01/12		2018/01/12		Rev	
2015/01/12		2018/01/12		1.0	

FAN CONN.

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			Document Number L14/L15 AND Gen2
			Date: Friday, January 22, 2021
			Sheet 90 of 128

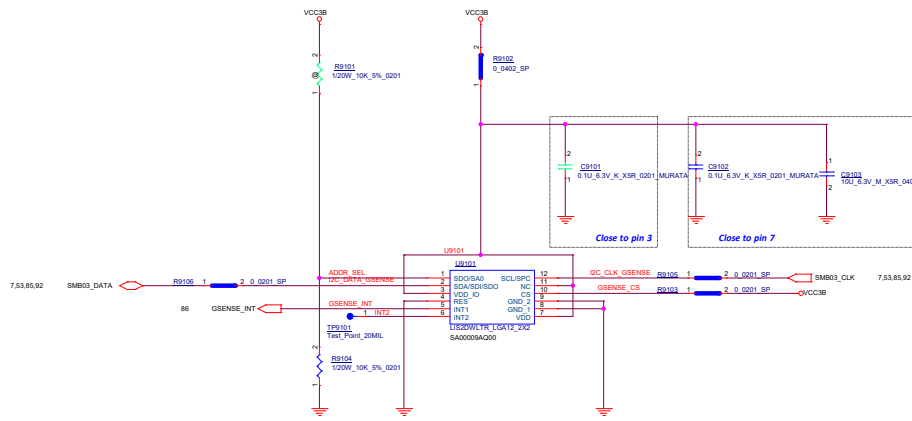



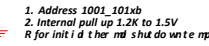
TABLE of G-Sensor (U9101)		
Vendor	P/N	LCFC P/N
ST	LIS2DWLTR	SA00009AQ00
BOSCH	BMA280	SA0000A1600

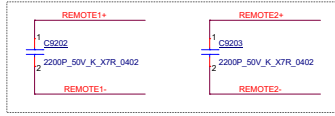
TABLE		
P/N	ADDR_SEL	Address
LIS2DWLTR	H	32h (W) & 33h (R)
	L	30h (W) & 31h (R)
BMA280	H	32h(W),33h(R)
	L	30h(W),31h(R)

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Size		C		Document Number		1.14/L15 AND Gen <sup>210</sup>	
Date		Friday, January 22, 2021		Sheet		91 of 108	

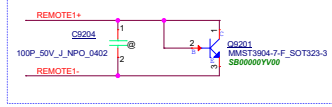
### Thermal Sensor



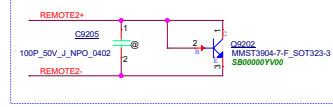
**Close to U9201**



**Close to CHARGER**

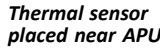


**Close to GPU**

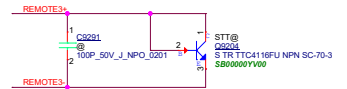
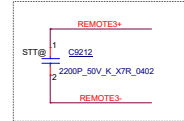


Trace width/space:10/10 mil  
Trace length:<8"


**Thermal sensor  
placed near APU**



*Close to U9202*



REMOTE+/- R, REMOTE1+/-, REMOTE2+/-:  
Trace width/space:10/10 mil  
Trace length:<8"

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Issued Date	2019/03/01	Deciphered Date	2019/07/23	<b>Thermal Sensor</b>	
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DATE	Friday, January 22, 2021		Sheet 15 of 15

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Scale	Document Number		Rev.
Other	L14/L15 AND Gen		0
DATE	Friday, January 22, 2021		Sheet 15 of 15

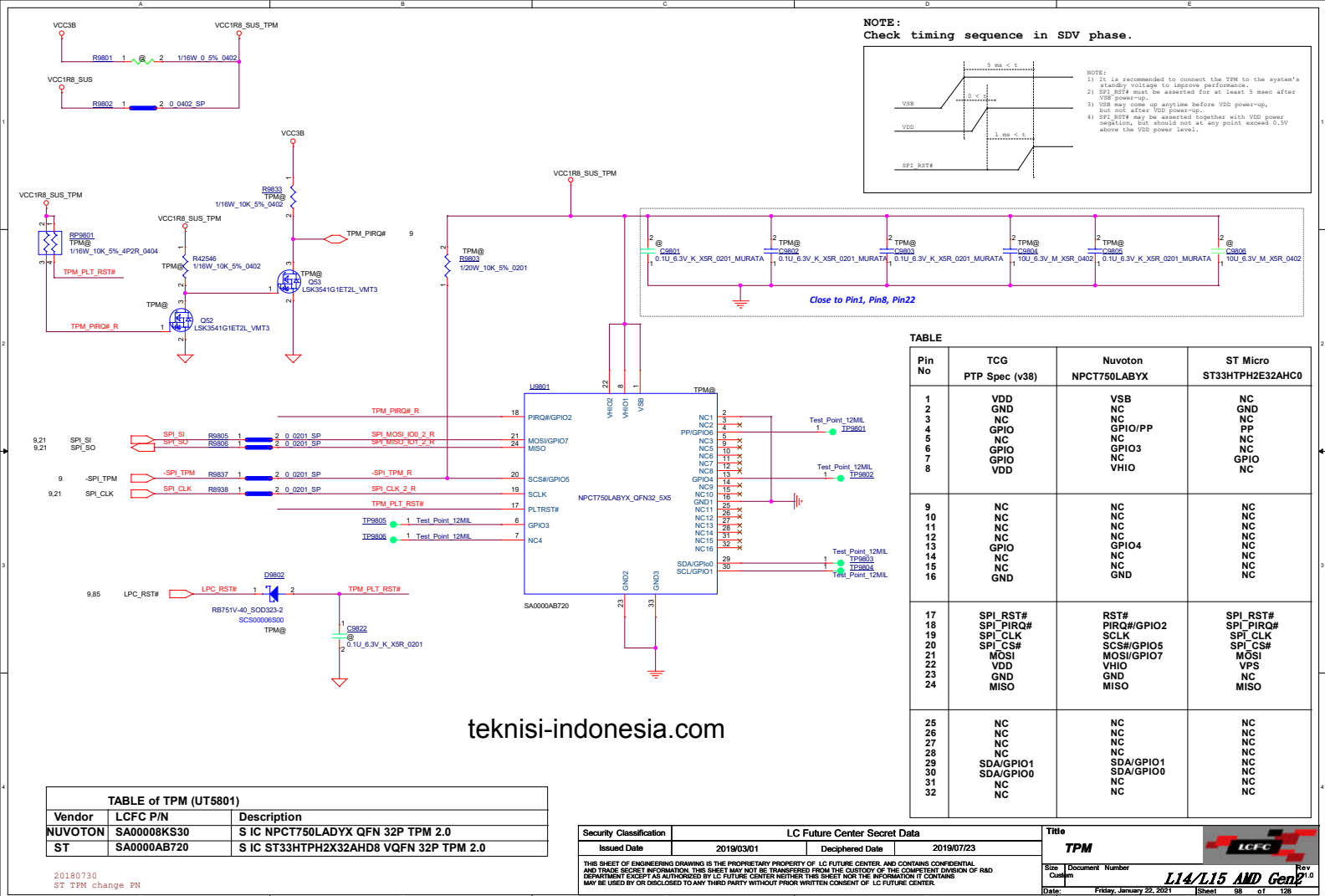
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ESEC Policy January 22, 2017			Issue 16 of 16




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Scale	Document Number		<b>L14/L15 AND Gen2</b>
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ESEC			Friday, January 22, 2021 15:00:00

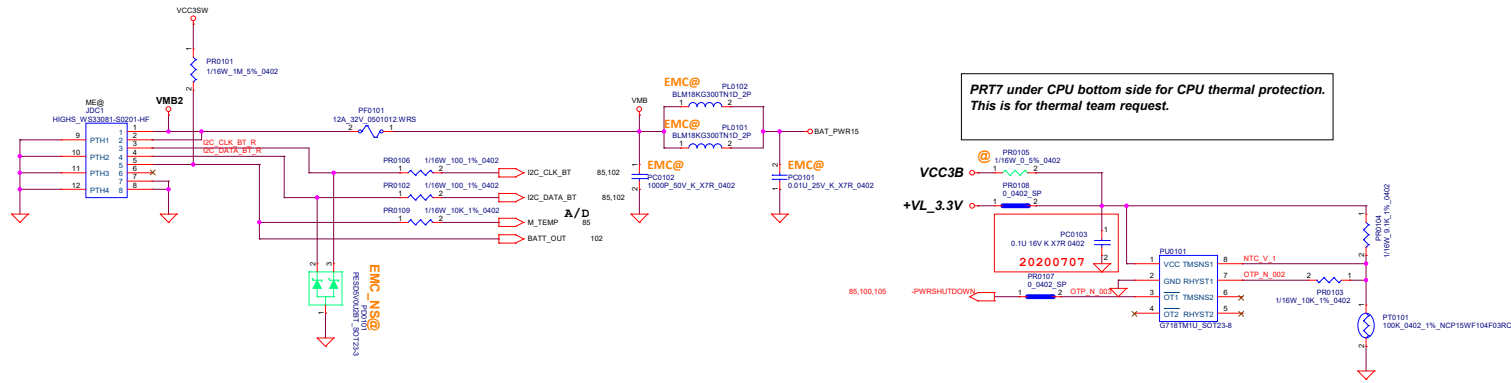



**For ME GND hole      Screw Hole**

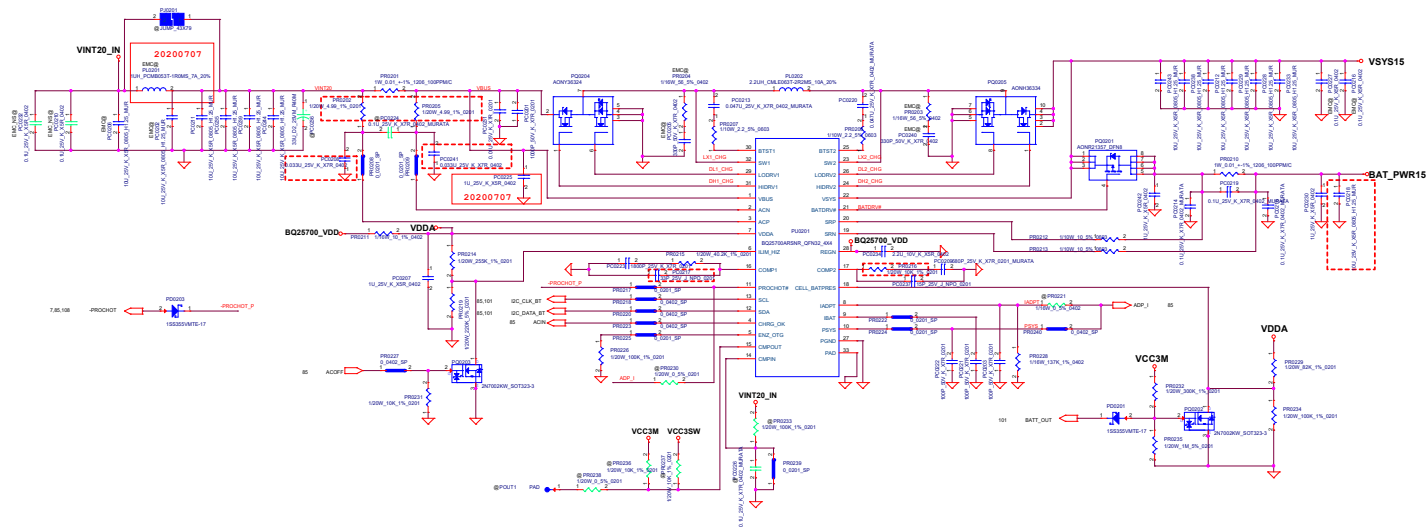


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Date	Friday, January 22, 2021		Issued		and Gen	

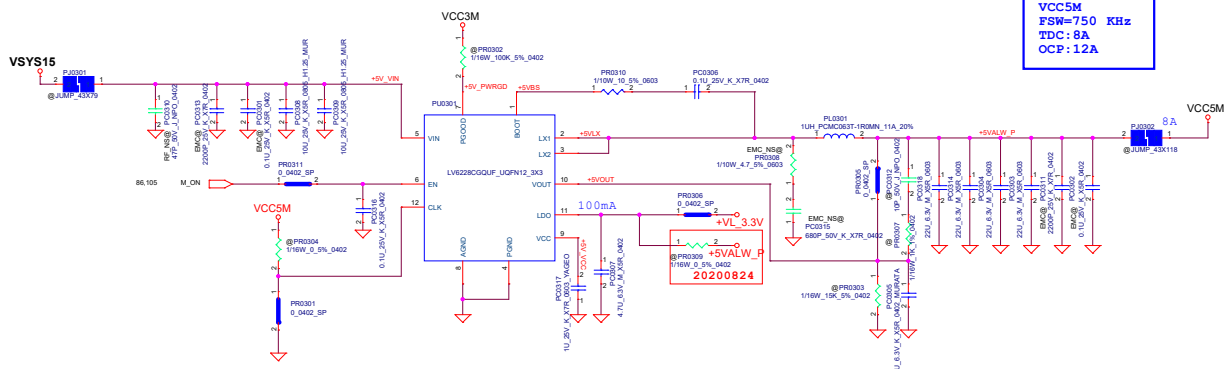





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Size	Document Number		L14/L15 AND		Rev
Customer					2.0
Date	Friday, January 22, 2021		Sheet	101	of 128

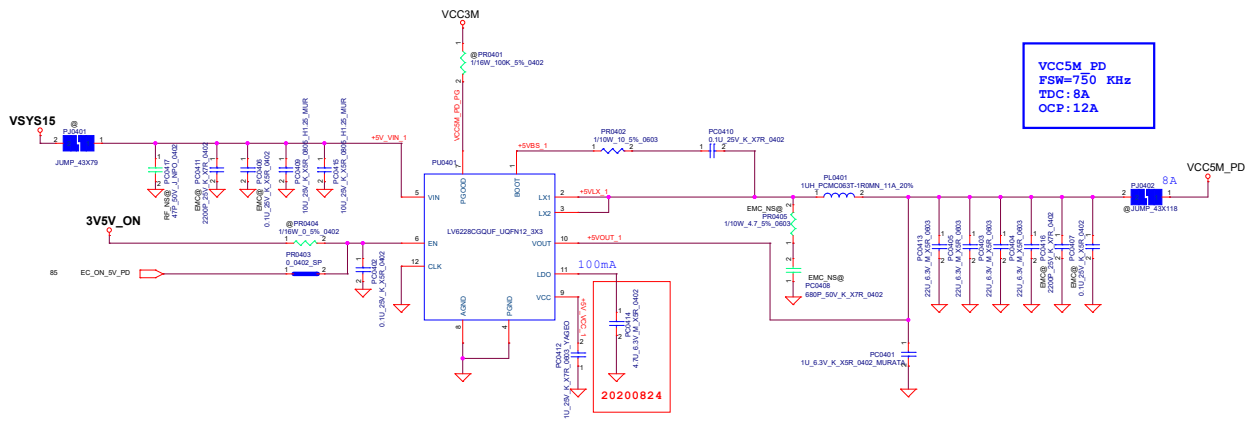


Title		BATTERY CHARGER(BQ25700A)			
Size	Document Number	L14/L15 AND		Rev 2.0	
Date	Friday, January 22, 2021	Sheet	102	of	178



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				Rev 2.0
				Date: Friday, January 22, 2011 Sheet 103 of 128

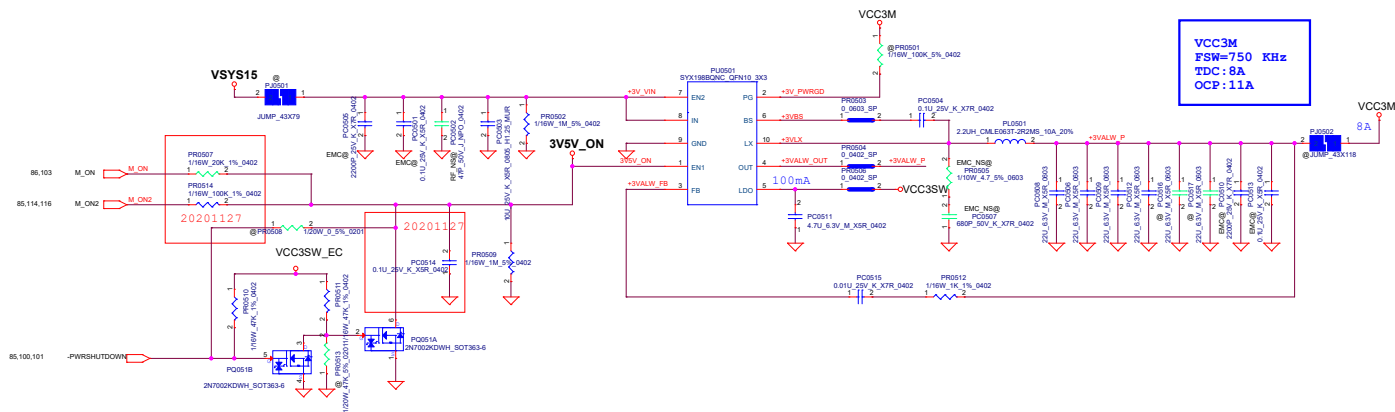
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VCC5M\_PD 59



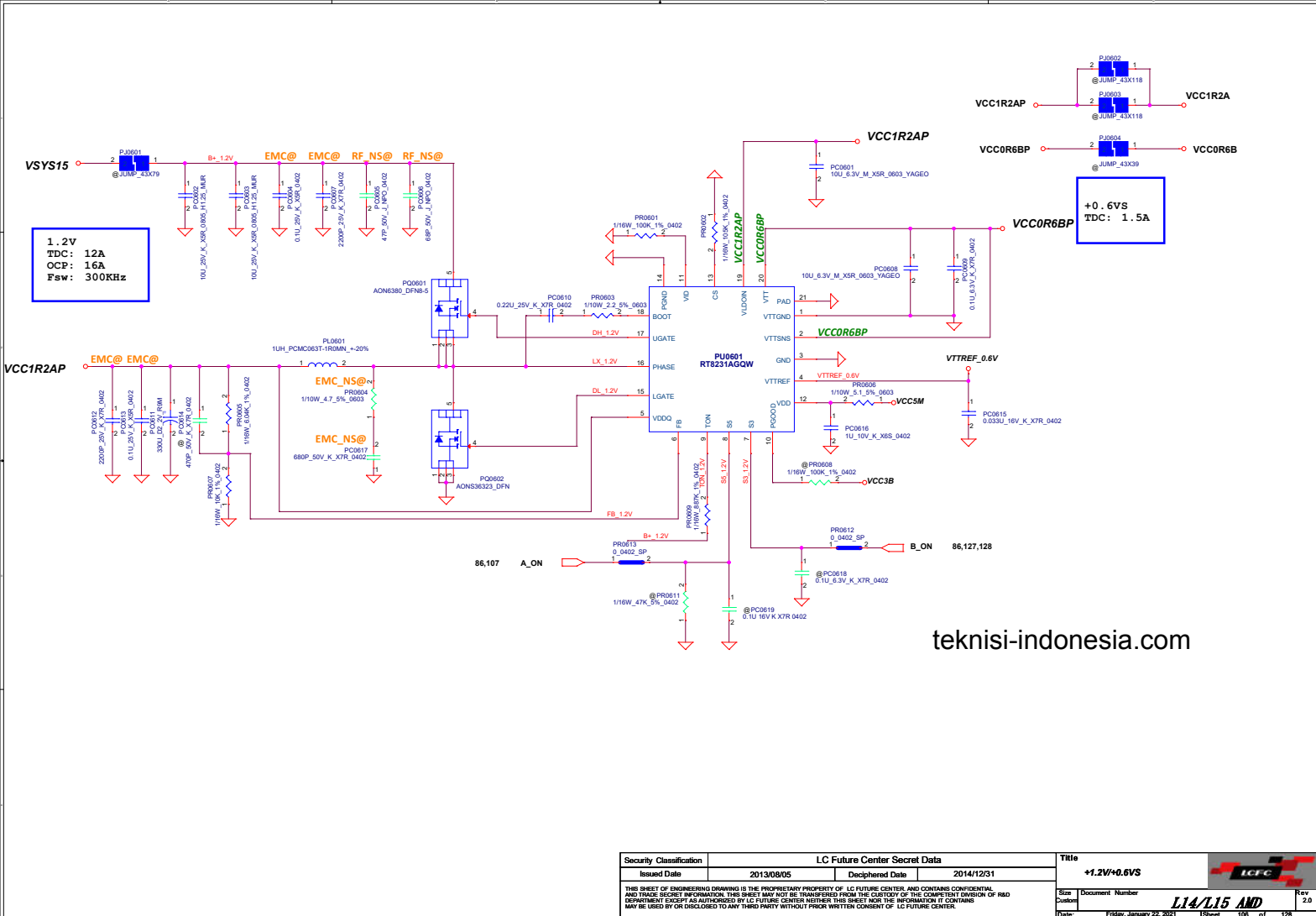
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Issued Date	2013/08/08	Declassified Date	2013/08/05	Size	Document Number
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				Date	Friday, January 22, 2011
				Sheet	94 of 138



VSYS15 51.84,76,100,102,103,104,106,108,109,110,114,116,128  
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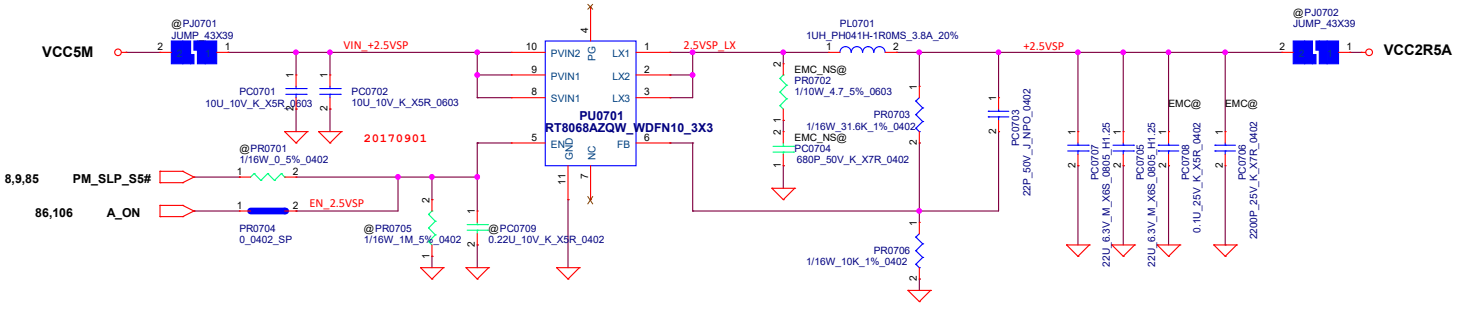
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Size	Document Number	114/115		Rev	2.0
Scale	Project Number	106-01		Sheet	106-01



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VCC5M 28,51,69,70,72,78,84,85,103,106,108,109,110,127,128  
VCC2R5A 33,34,35,36

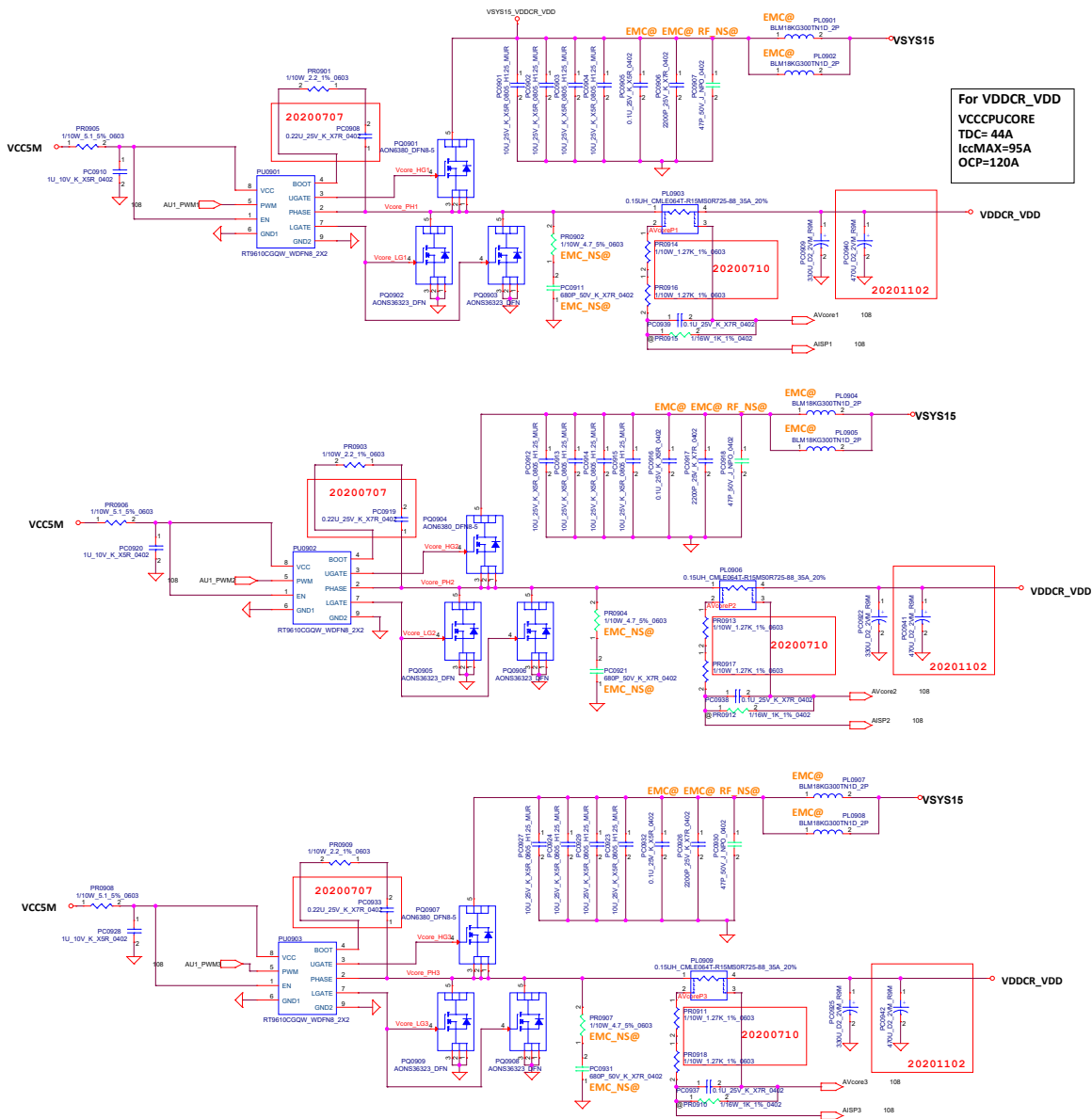
VCC2R5A  
TDC: 2A  
OCP: 4A  
Fsw: 1MHz



Security Classification		LC Future Center Secret Data		Title	
Issued Date	2013/08/05	Deciphered Date	2014/12/31	DC/DC VCC2R5A(RT8068A)	
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				Date: Friday, January 22, 2021	Rev 2.0
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Issue Date	Friday, January 23, 2015			18 of 13




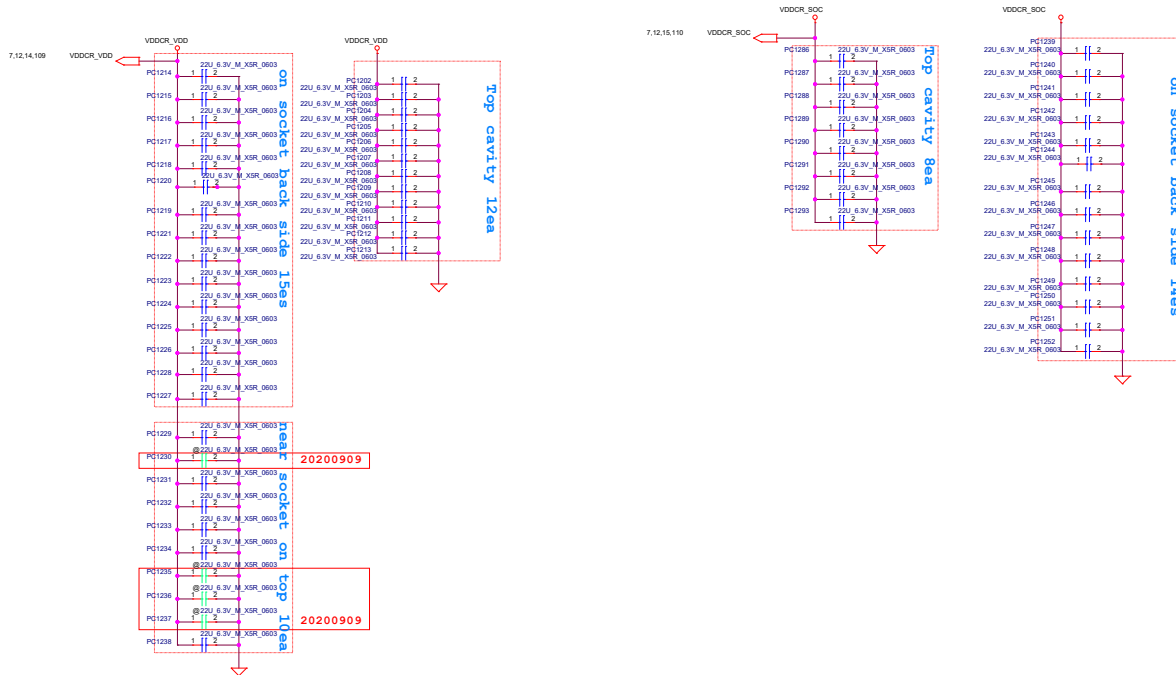
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Issued Date	2013/08/05	Deciphered Date	2014/12/31	Size		
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				Date:	Friday, January 22, 2021	2.0
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C				2.1	
Date	Friday, January 24, 2014		Sheet	115 of 128	

VSYS15 51,64,76,100,102,103,104,105,106,108,109,110,116,128

VCCR1R35VIDEO VCCR1R35VIDEO

NB691\_VCC0R75

VDD0R75  
FSW=700KHz  
TDC: 4A  
OCP: 7.2A


VSYS15

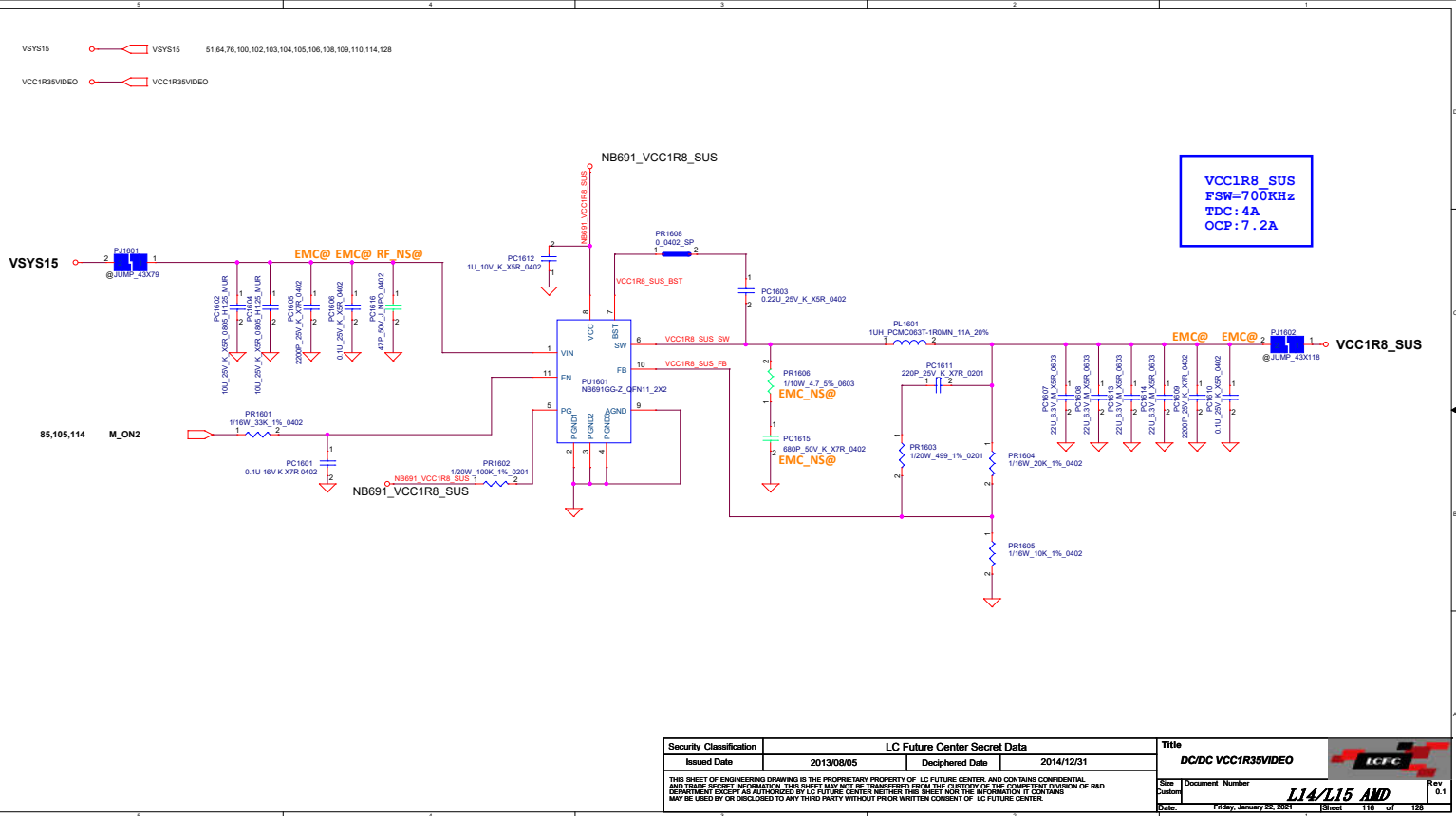
85,105,116 M\_ON2

VDD0R75


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				Date:	Friday, January 22, 2021
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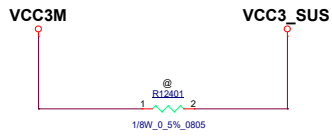
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D				D																																			
C				C																																			
B				B																																			
A				A																																			
<table><tr><td>Security Classification</td><td colspan="3">LC Future Center Secret Data</td><td>Title</td></tr><tr><td>Issued Date</td><td>2015/01/12</td><td>Deciphered Date</td><td>2016/01/12</td><td>LOADSW VCCIO&amp;VCCST&amp;VCCST</td></tr><tr><td colspan="4">THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&amp;D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.</td><td>Size Custom</td></tr><tr><td colspan="4"></td><td>Document Number <b>L14/L15 AND</b></td></tr><tr><td colspan="4"></td><td>Date: Friday, January 22, 2021</td></tr><tr><td colspan="4"></td><td>Sheet 123 of 128</td></tr><tr><td colspan="4"></td><td>Rev 1.0</td></tr></table>					Security Classification	LC Future Center Secret Data			Title	Issued Date	2015/01/12	Deciphered Date	2016/01/12	LOADSW VCCIO&VCCST&VCCST	THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.				Size Custom					Document Number <b>L14/L15 AND</b>					Date: Friday, January 22, 2021					Sheet 123 of 128					Rev 1.0
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C				1.0	
Date	Friday, January 24, 2014		Sheet	126 of 128	

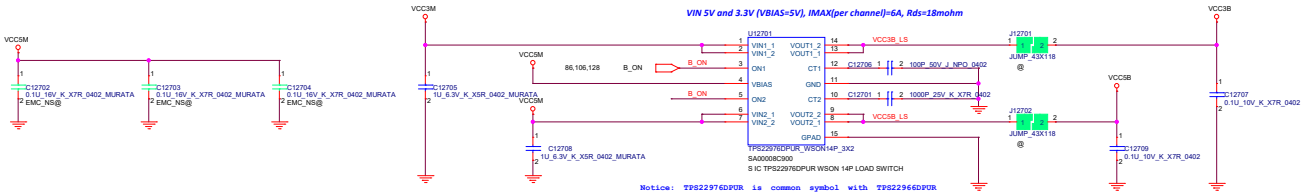
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A									

VCC3BW		VCC3SW	20,51,59,85,101,102,105
VCC3M		VCC3M	8,9,10,12,22,23,28,51,57,59,64,66,67,73,76,78,84,85,86,88,89,102,103,104,105,108,124
VCC5M		VCC5M	28,51,69,70,72,78,84,85,103,106,107,108,109,110,128
VCC5B		VCC5B	51,54,72,88,90
VCC3B		VCC3B	7,8,9,12,28,33,35,51,53,59,64,67,70,73,78,85,88,89,91,92,98,101,106



1. MIRROR code, is correct????  
2. After reset EC, EC control "Low", not High or Disable.

Smart Switch  
VCC5M To VCC5B  
VCC3M To VCC3B

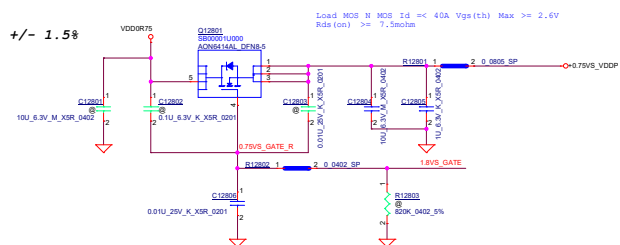


Notice: TPS22976DPUR is common symbol with TPS22966DPUR

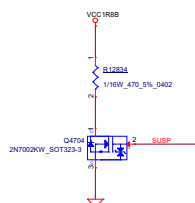
TABLE of POWER SWITCH (U7201)		
Vendor	LCFC P/N	Description
TI	SA00008C900	S IC TPS22976DPUR WSON 14P LOAD SWITCH
GMT	SA00008F400	S IC G2898KD1U TDFN 14P LOAD SWITCH

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**VDD0R75 to +0.75VDDP 10A request**  
V9B+ 9V--13V

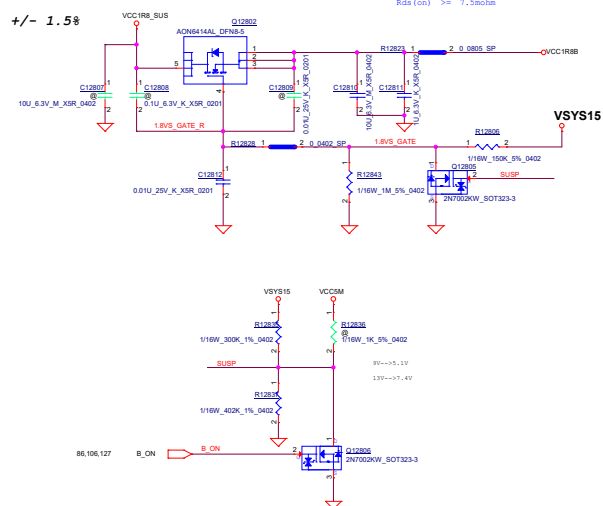



**For DisCharge**



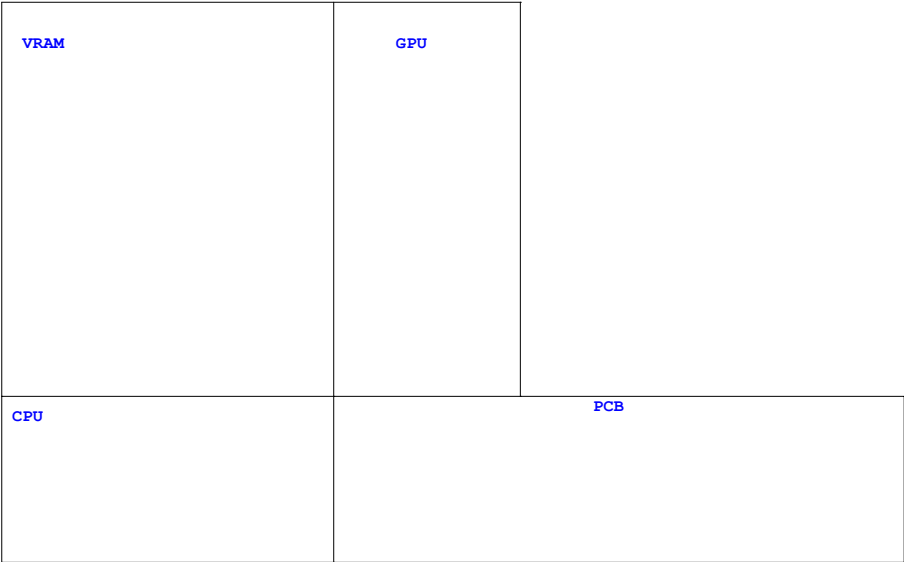
### VCC1R8B load Switch VCC1R8\_SUS to VCC1R8B 2.7A request

Load MOS N MOS Id <= 40A Vgs(th) Max >= 2.6V  
Rds(on) >= 7.5mohm



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Origin			
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Title			
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Size	Document Number	Rev	
B		1.0	
Date:		Sheet 129 of 129	
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